FIG. 1

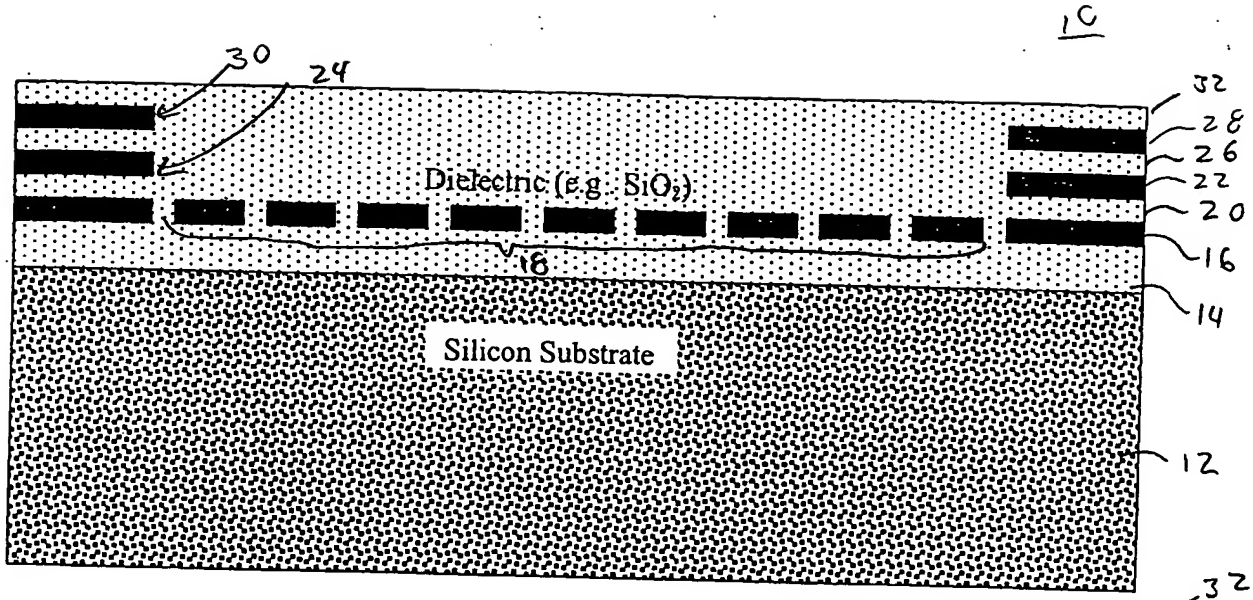


FIG. 2

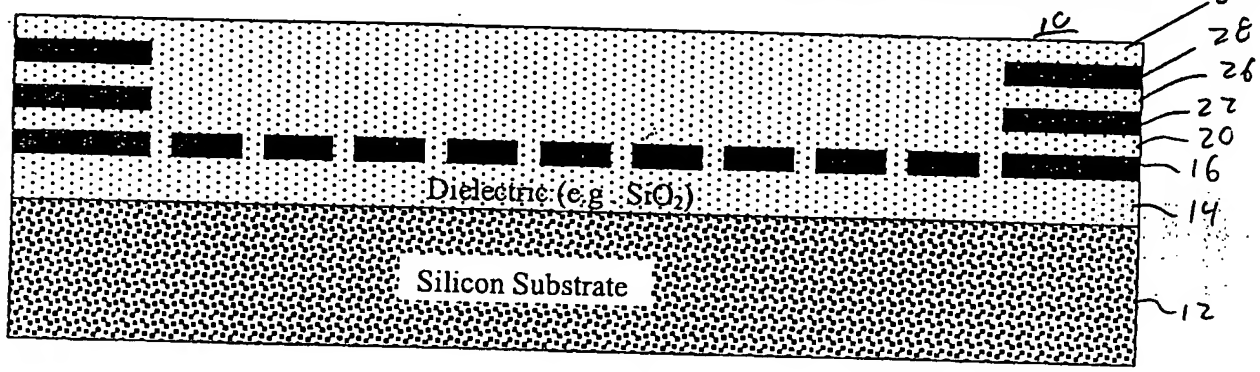


FIG. 3

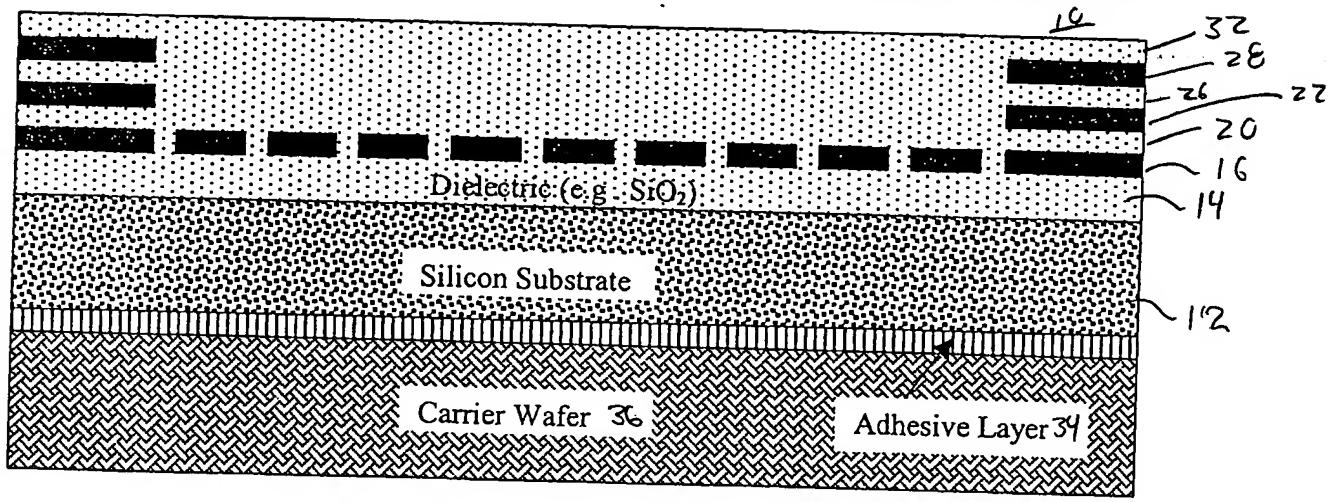


FIG. 4

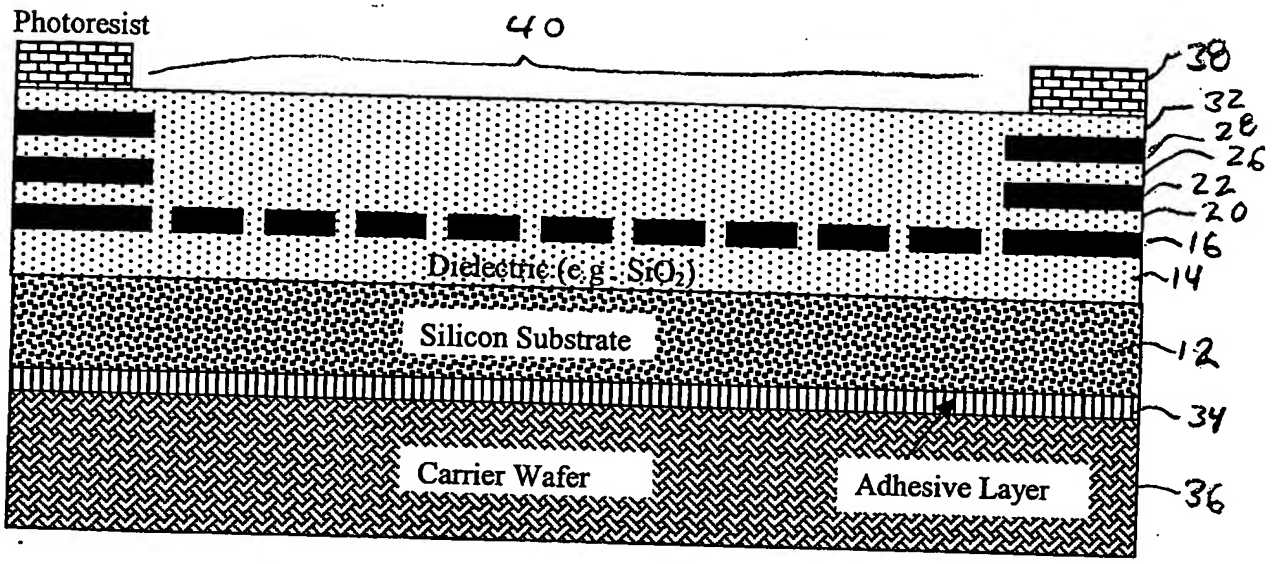

Photoresist
40
38
32
28
26
22
20
16
14
Dielectric (e.g. SiO_2)
Silicon Substrate
12
34
Carrier Wafer
Adhesive Layer
36

FIG. 5

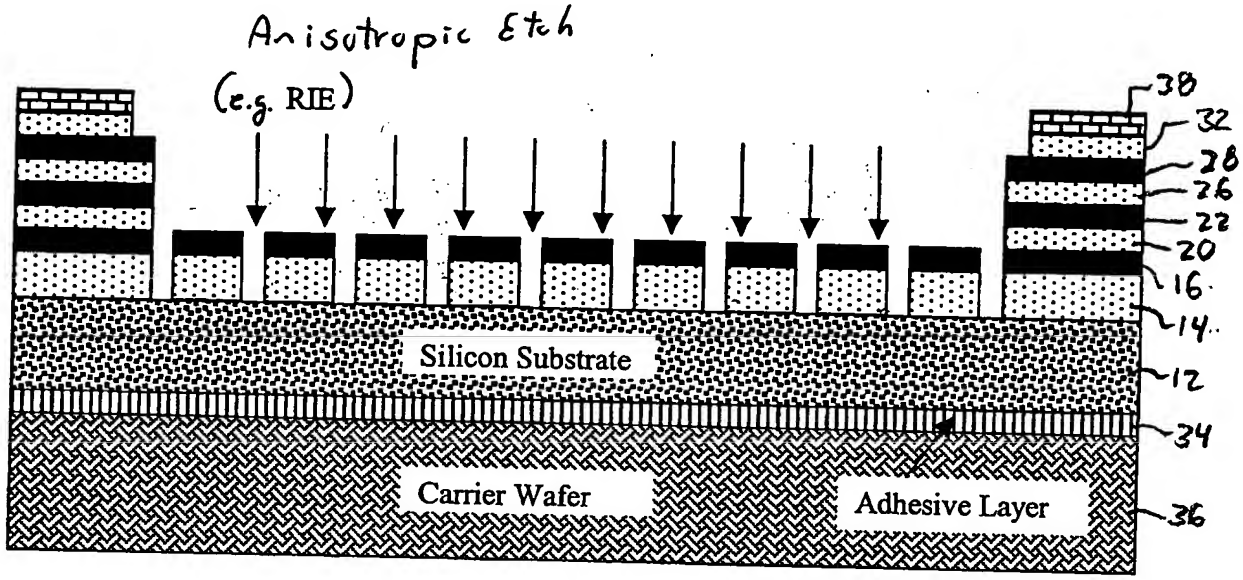

Anisotropic Etch
(e.g. RIE)
38
32
28
26
22
20
16
14
Silicon Substrate
12
34
Carrier Wafer
Adhesive Layer
36

FIG. 6

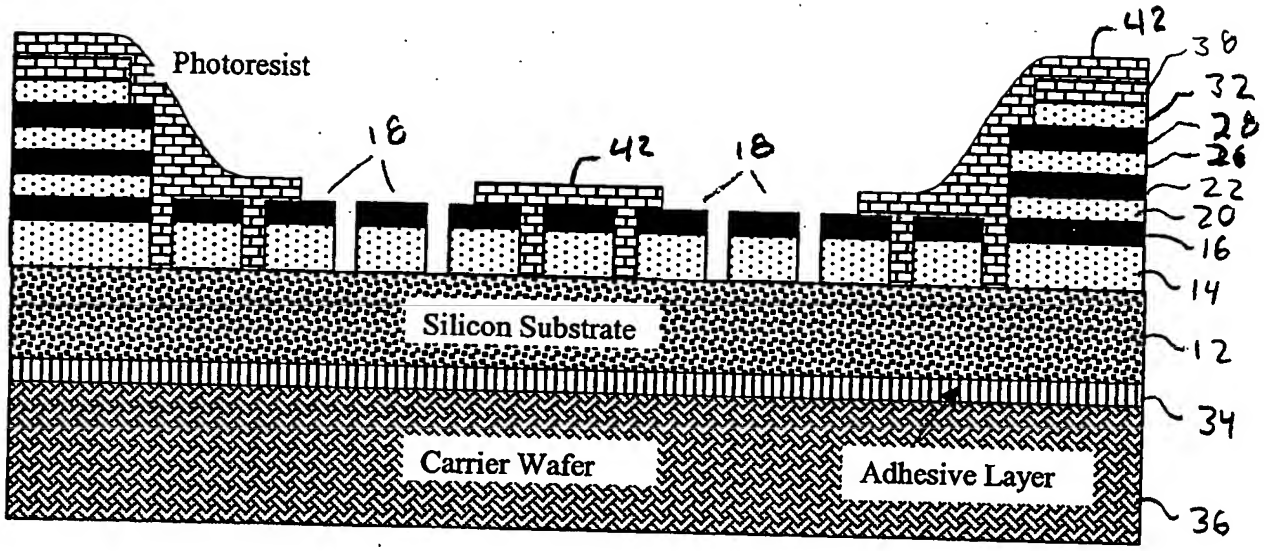

Photoresist
18
42
18
42
38
32
28
26
22
20
16
14
Silicon Substrate
12
34
Carrier Wafer
Adhesive Layer
36

FIG. 7

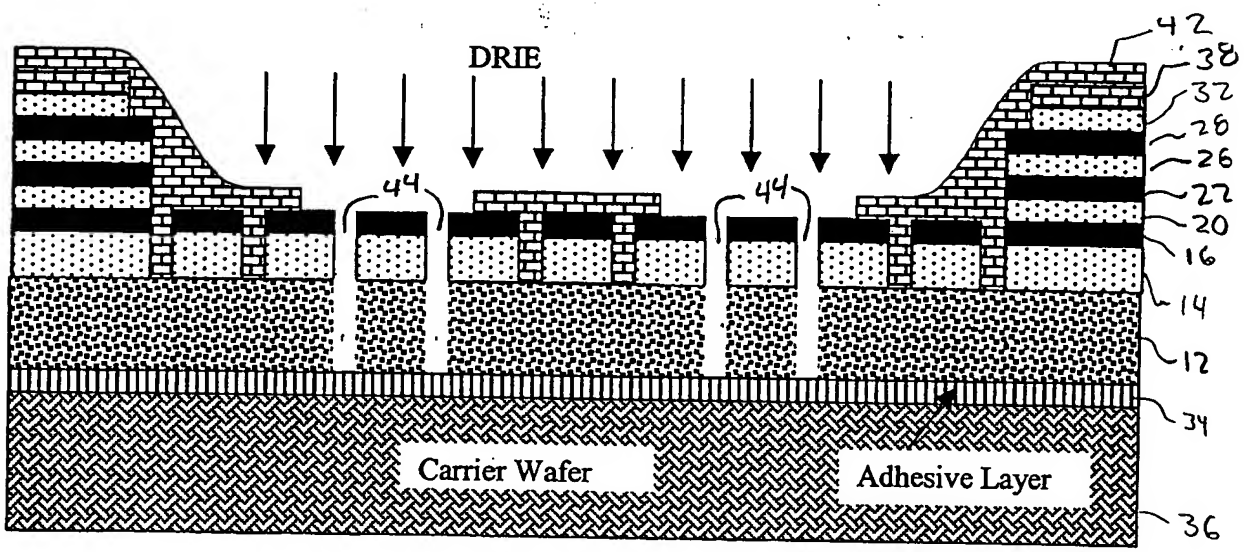

DRIE
44
44
42
38
32
28
26
22
20
16
14
12
34
Carrier Wafer
Adhesive Layer
36

FIG. 8

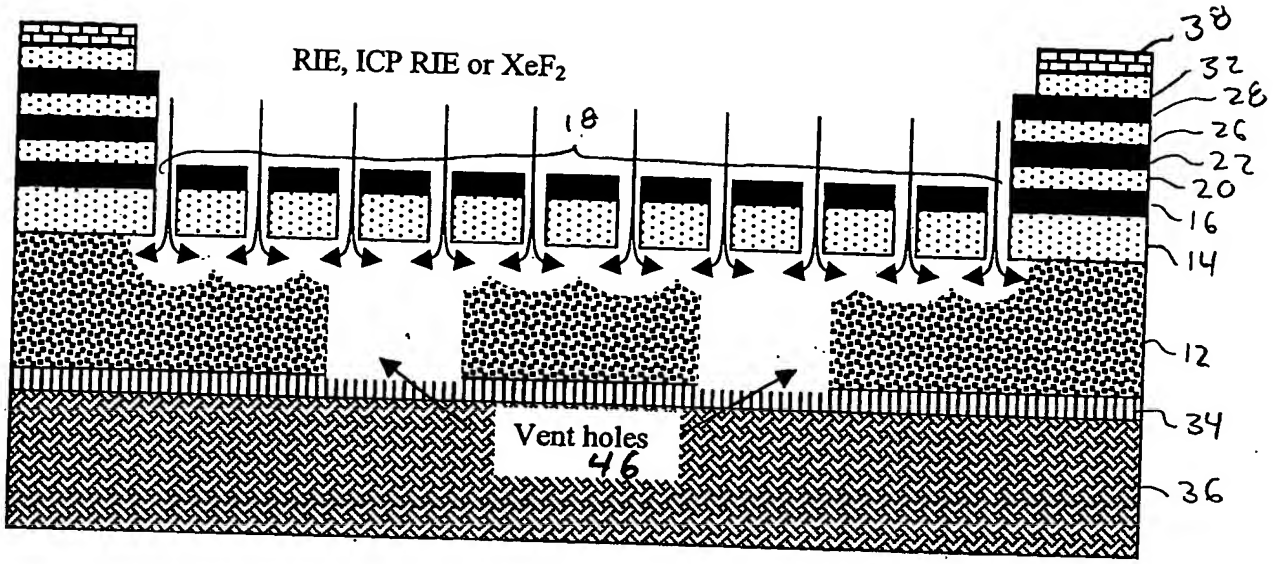


FIG. 9

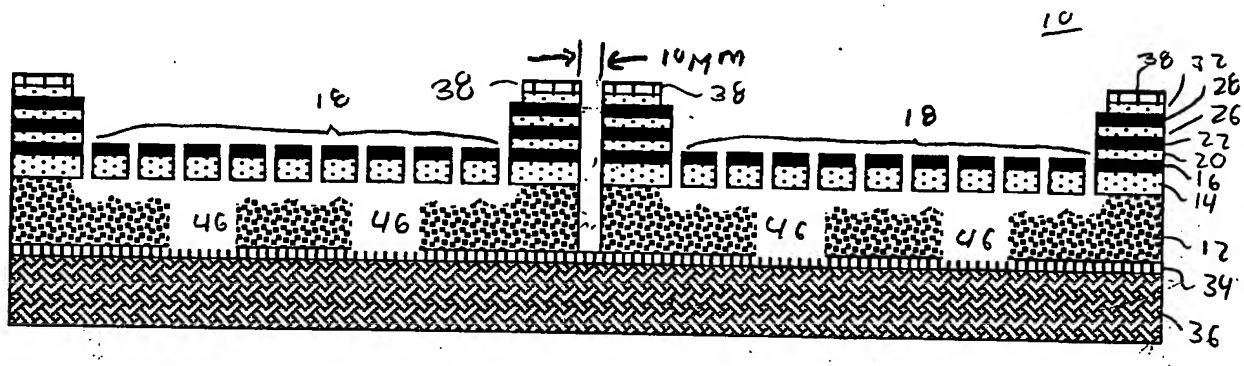
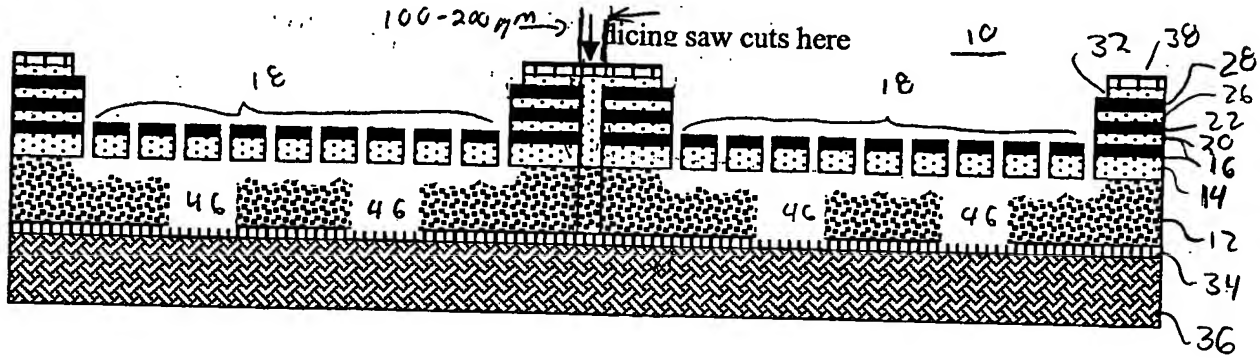


FIG. 10



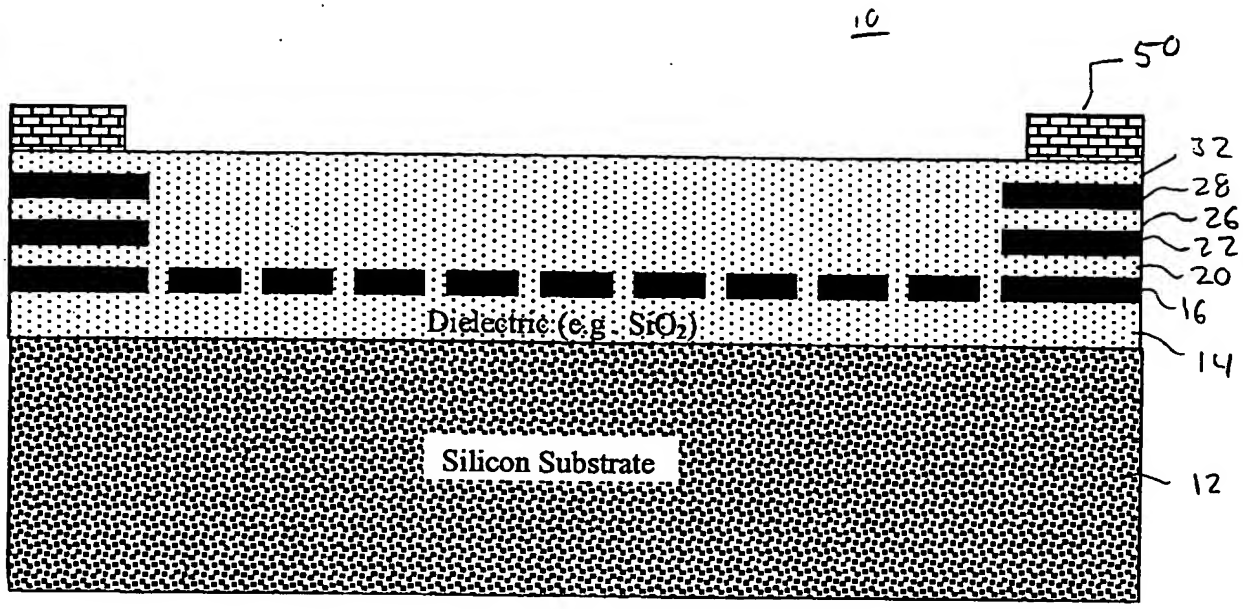


FIG. 11

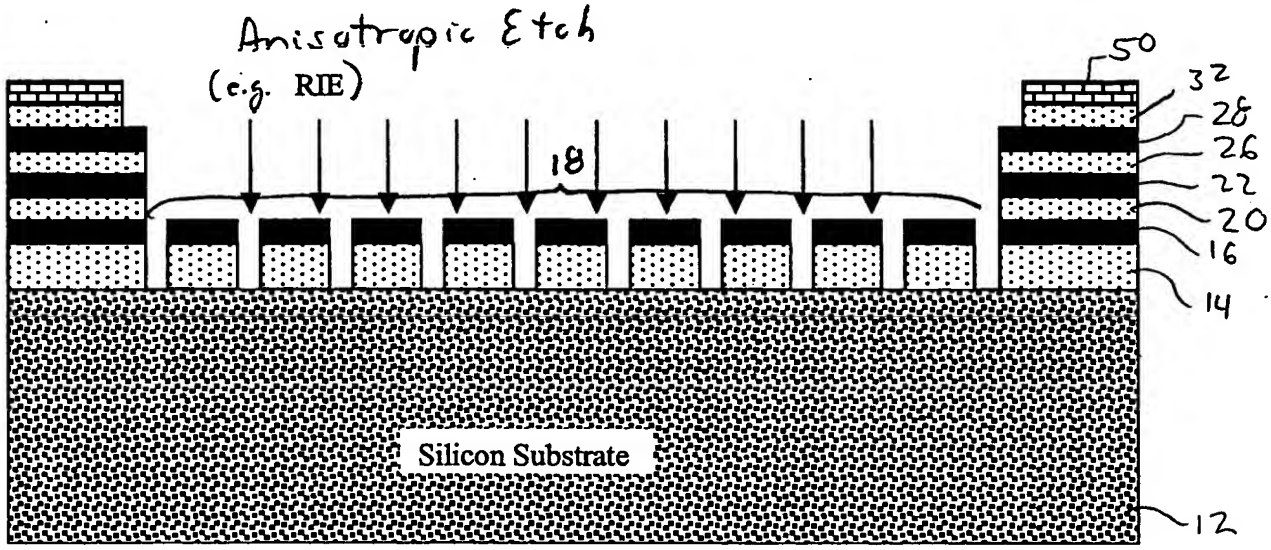


FIG. 12

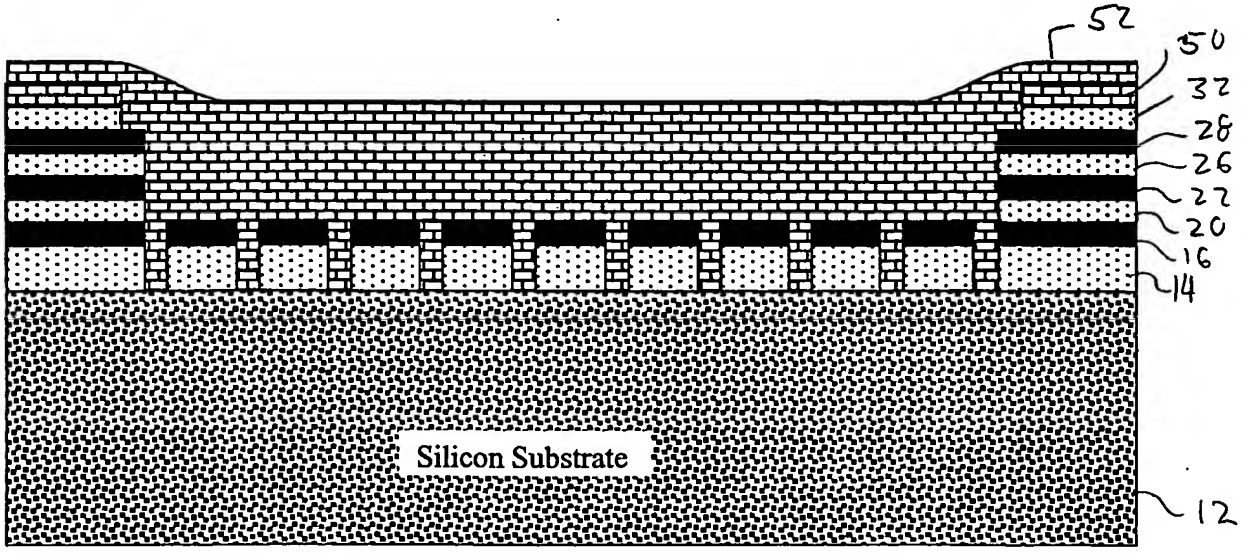


FIG. 13

FIG. 14

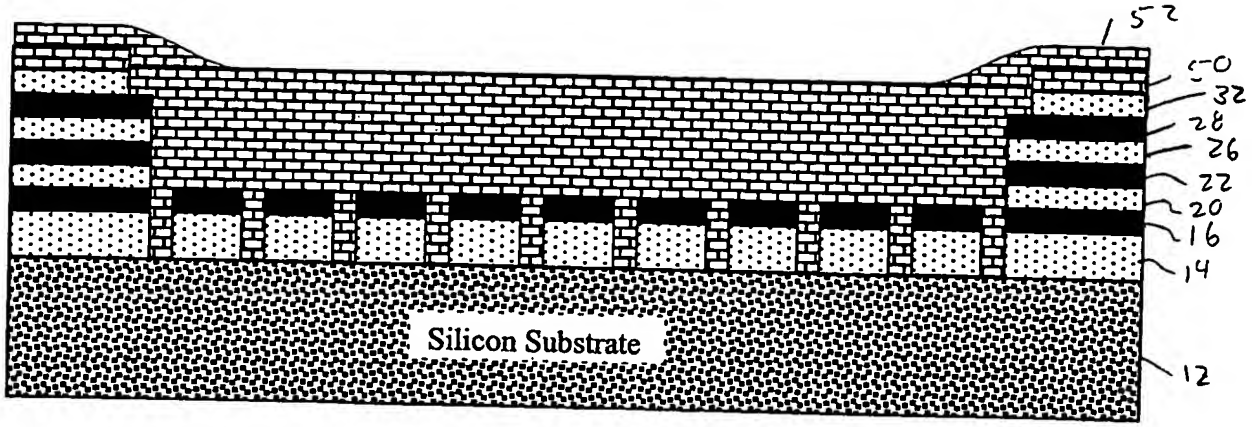
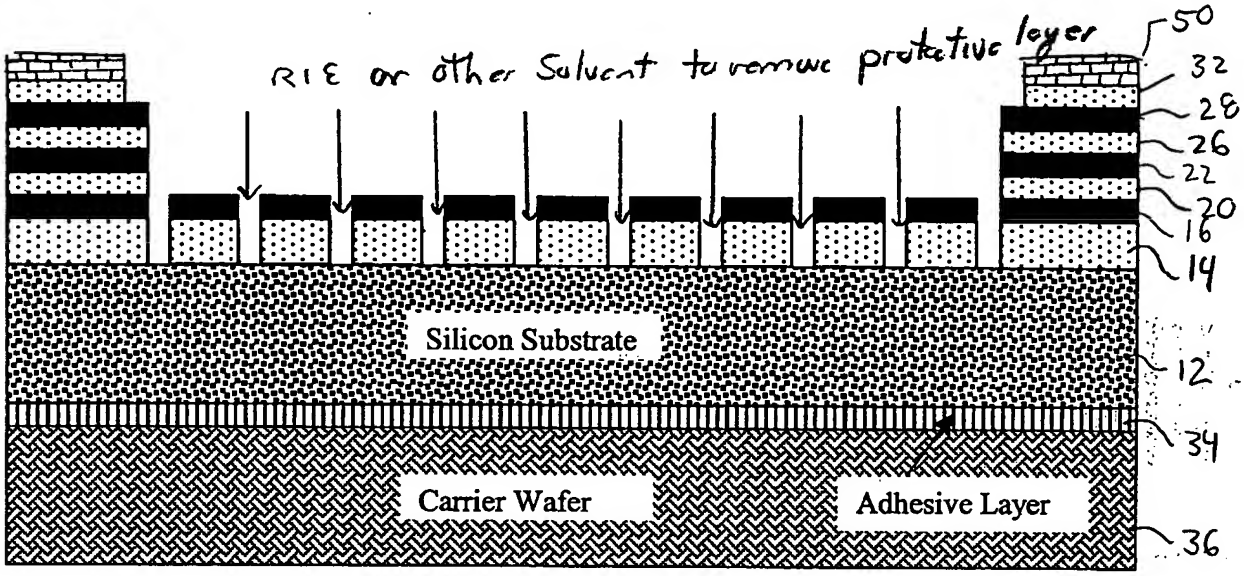

52
50
32
28
26
22
20
16
14
Silicon Substrate
12

FIG. 15


RIE or other Solvent to remove protective layer
50
32
28
26
22
20
16
14
Silicon Substrate
12
34
Carrier Wafer
Adhesive Layer
36

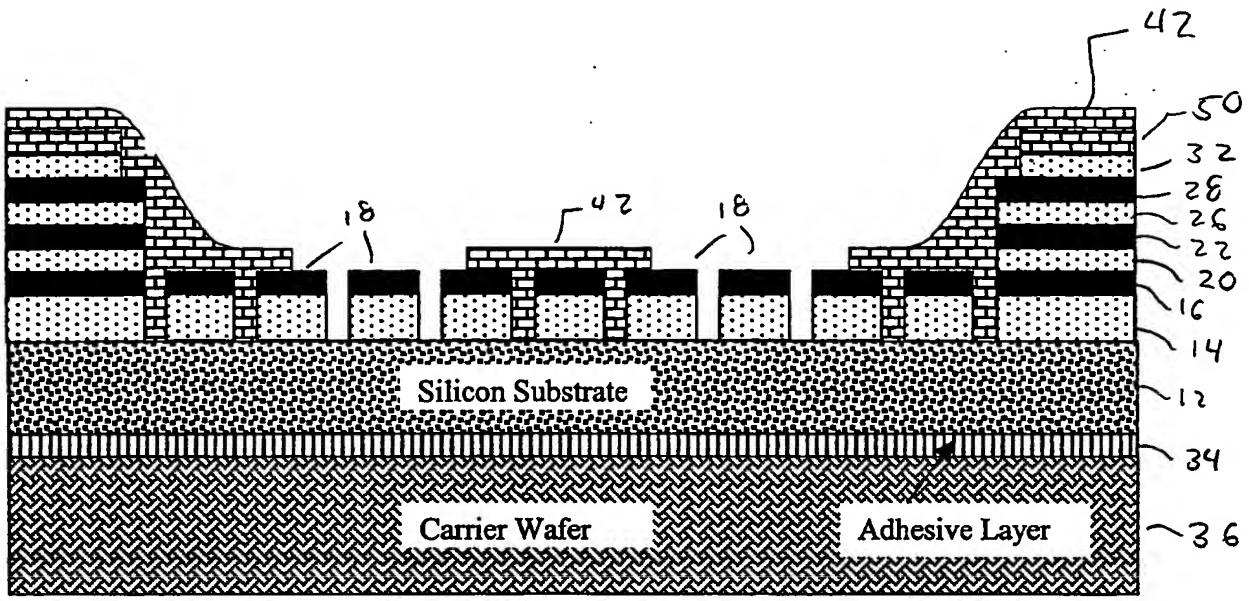

42
50
32
28
26
22
20
16
14
18
42
18
Silicon Substrate
12
34
Carrier Wafer
Adhesive Layer
36

FIG 16.

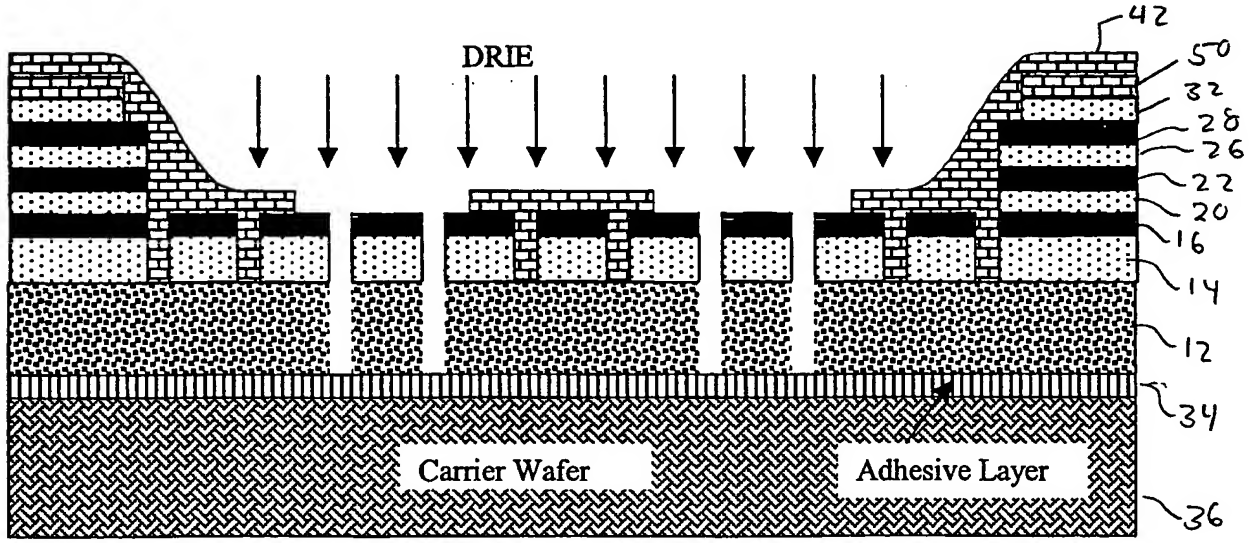

42
DRIE
50
32
28
26
22
20
16
14
12
34
Carrier Wafer
Adhesive Layer
36

FIG. 17

FIG. 18

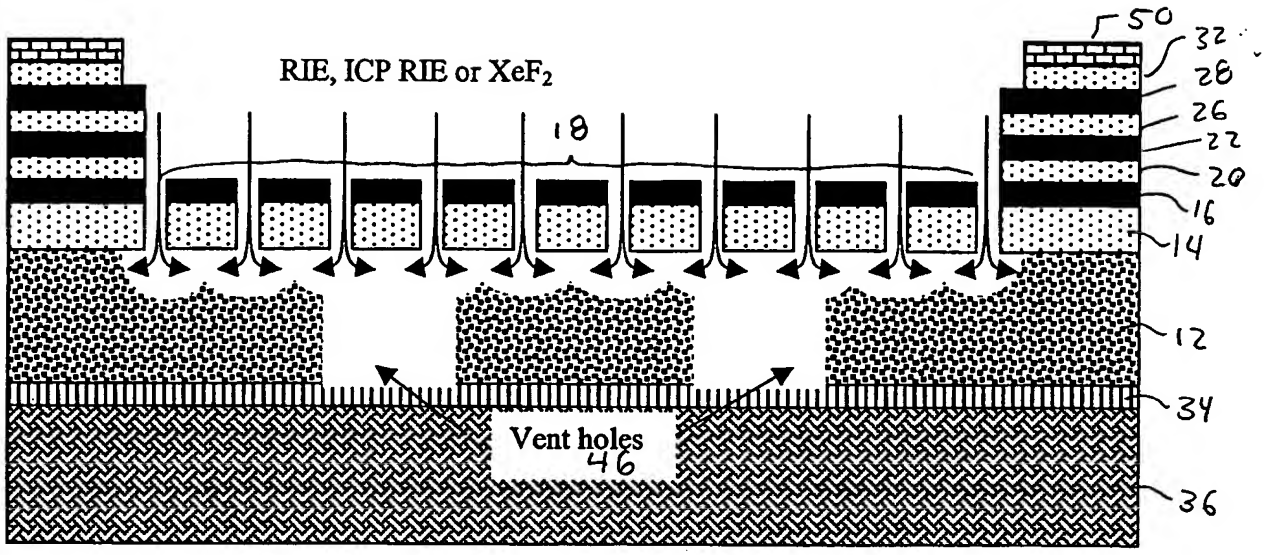

RIE, ICP RIE or XeF_2
50
32
28
26
22
20
18
16
14
12
34
Vent holes
46
36

FIG. 19

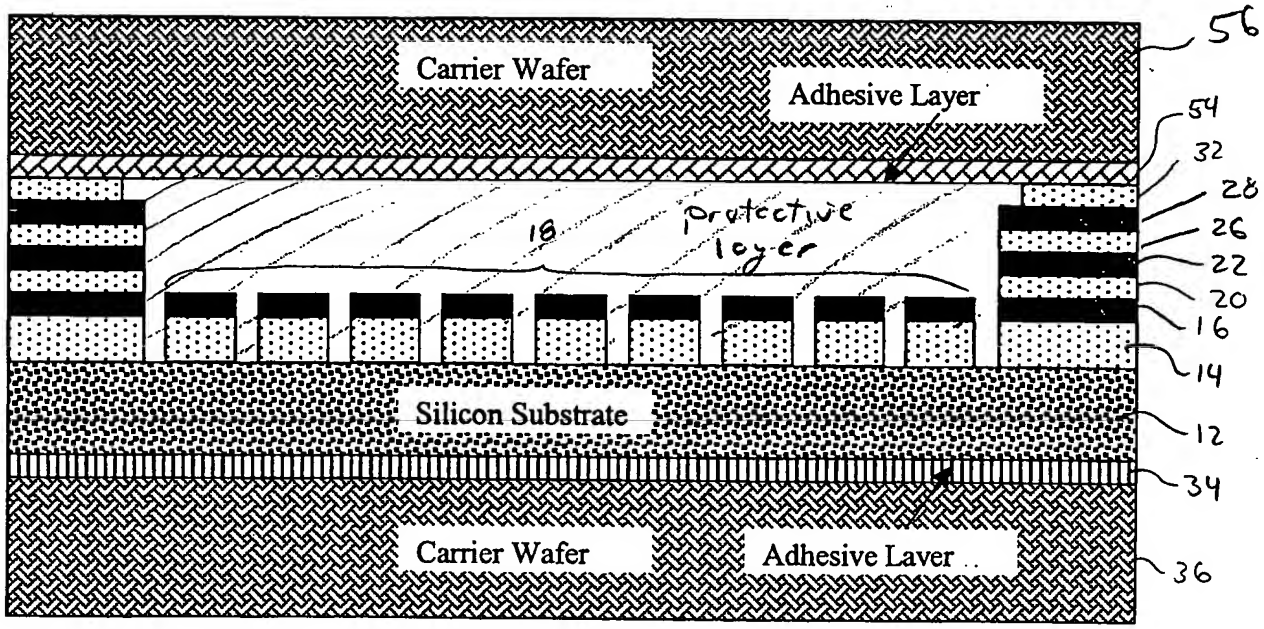

56
Carrier Wafer
Adhesive Layer
54
32
28
26
22
20
18
protective layer
16
14
Silicon Substrate
12
34
Carrier Wafer
Adhesive Laver
36

FIG. 20

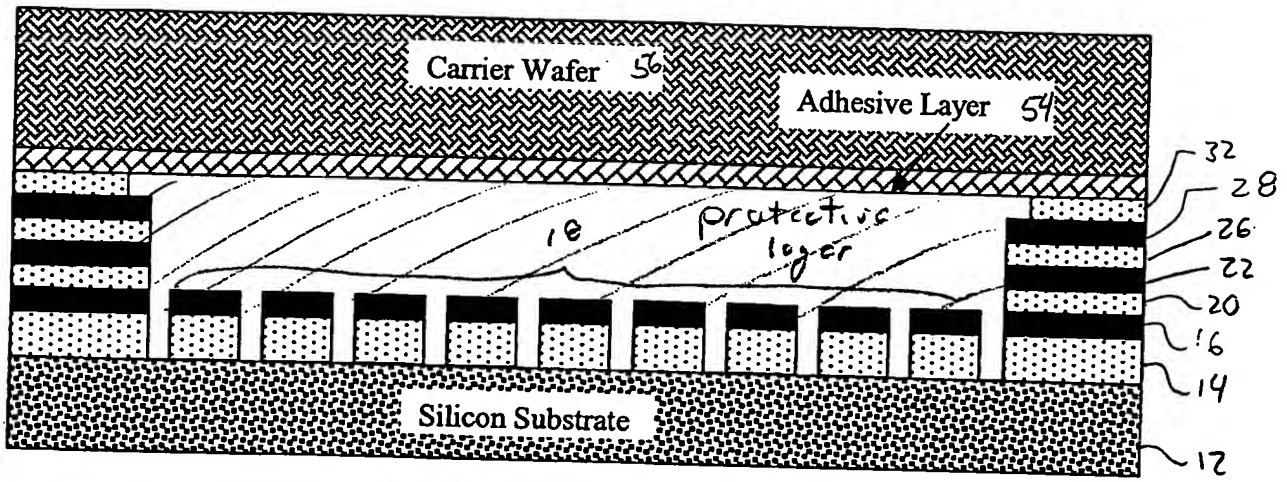


FIG. 21

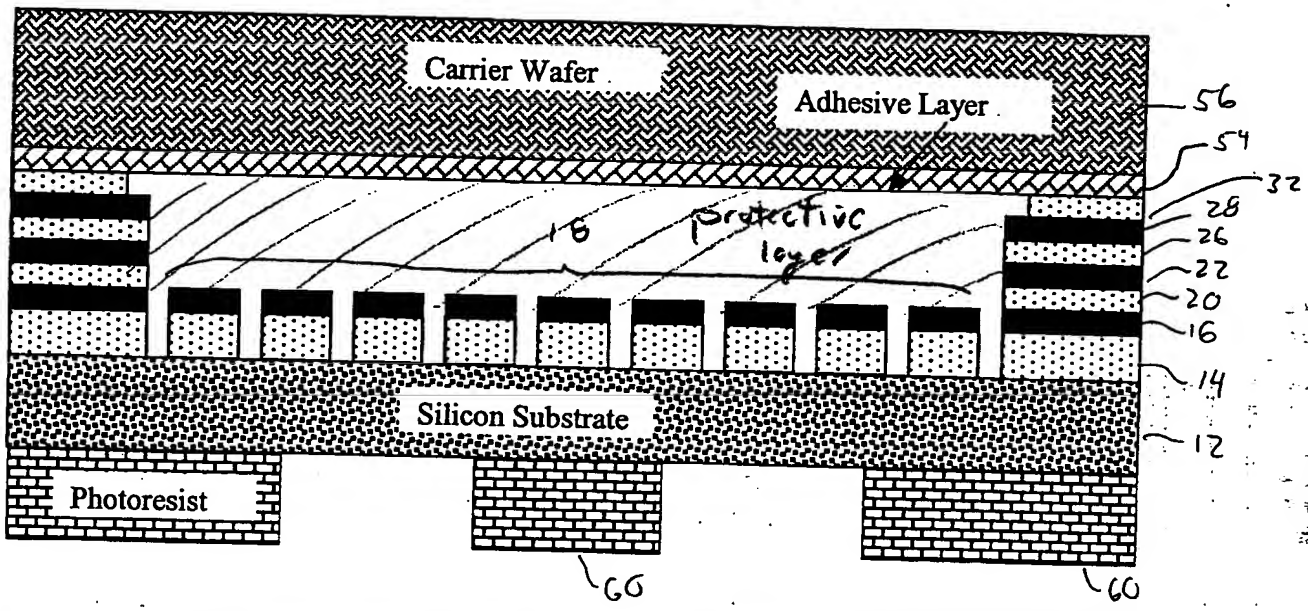


FIG. 22

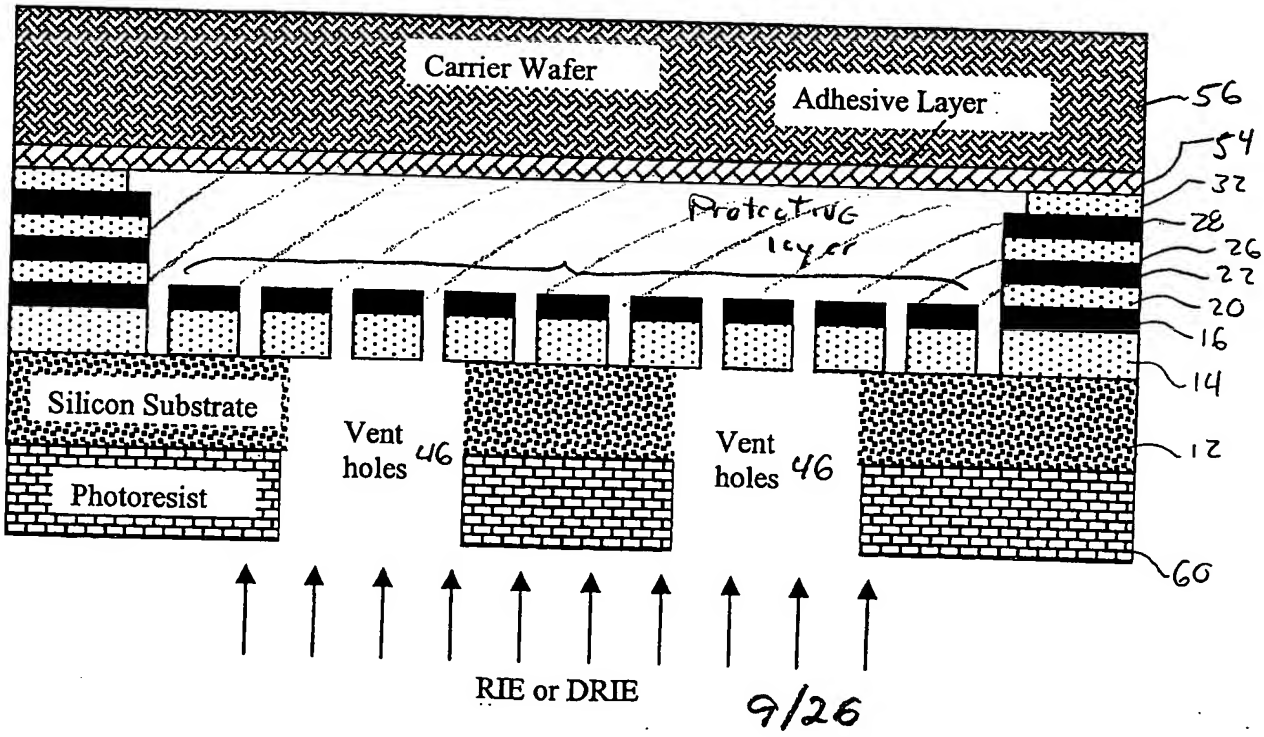


FIG. 23

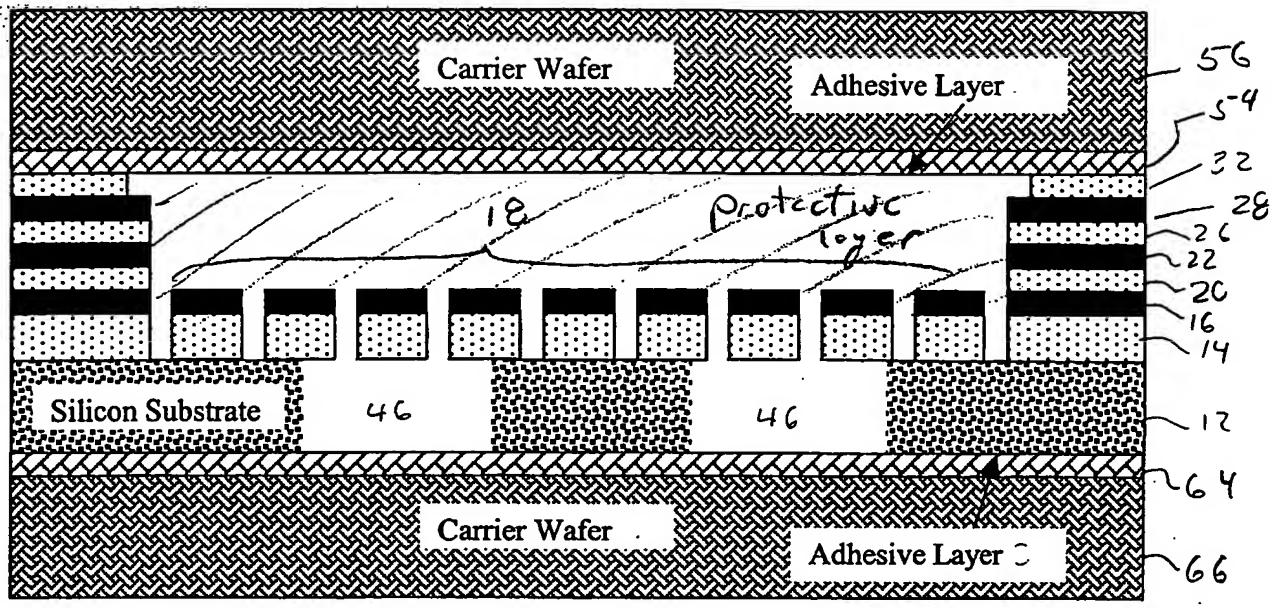


FIG. 24

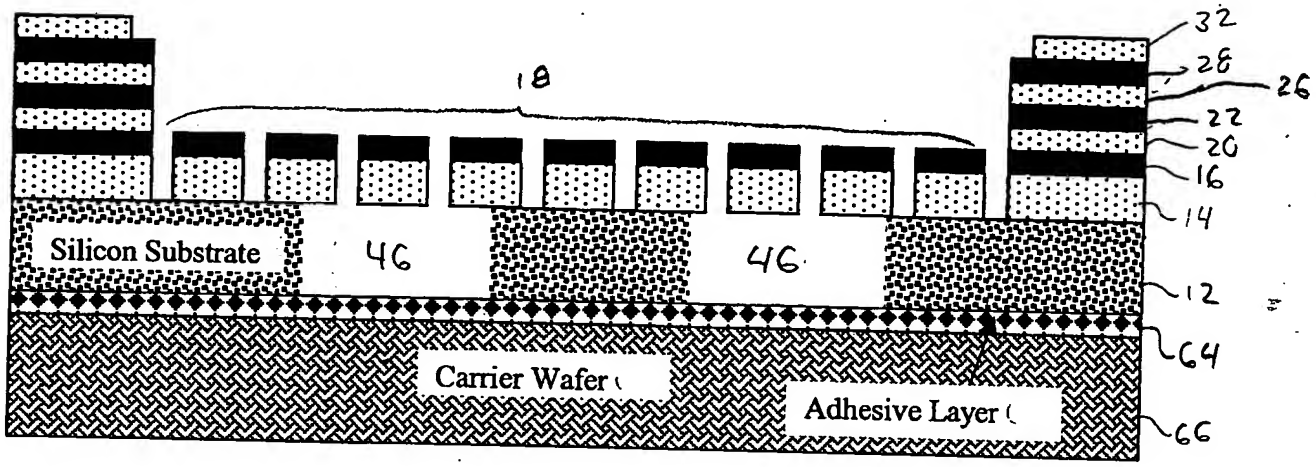


FIG. 25

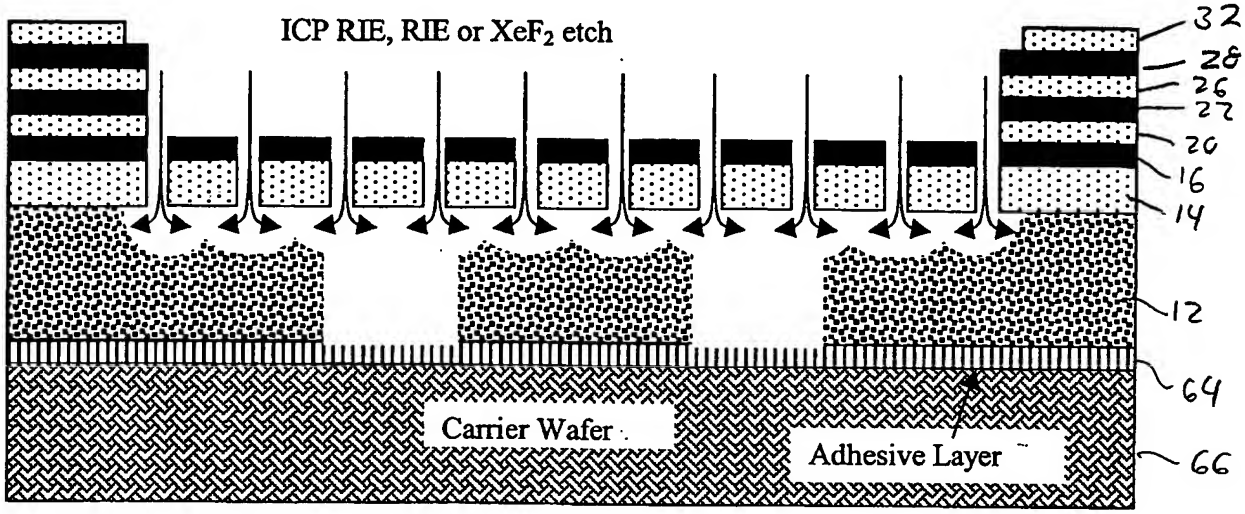


FIG. 26

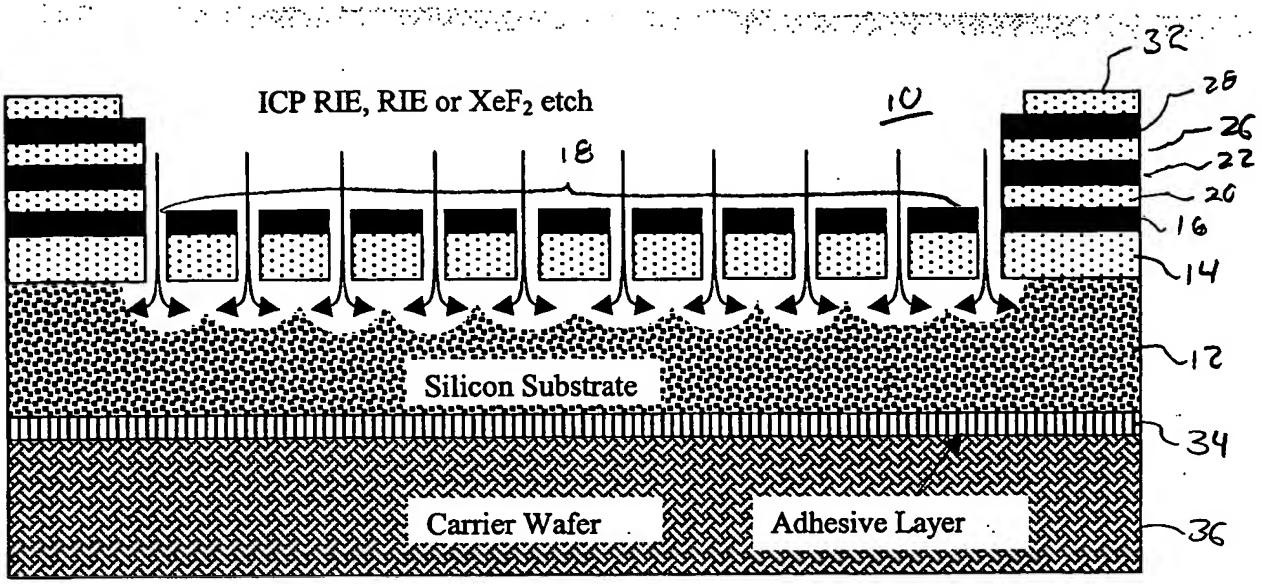

ICP RIE, RIE or XeF_2 etch
10
32
28
26
22
20
16
14
18
12
Silicon Substrate
34
Carrier Wafer
Adhesive Layer
36

FIG. 27

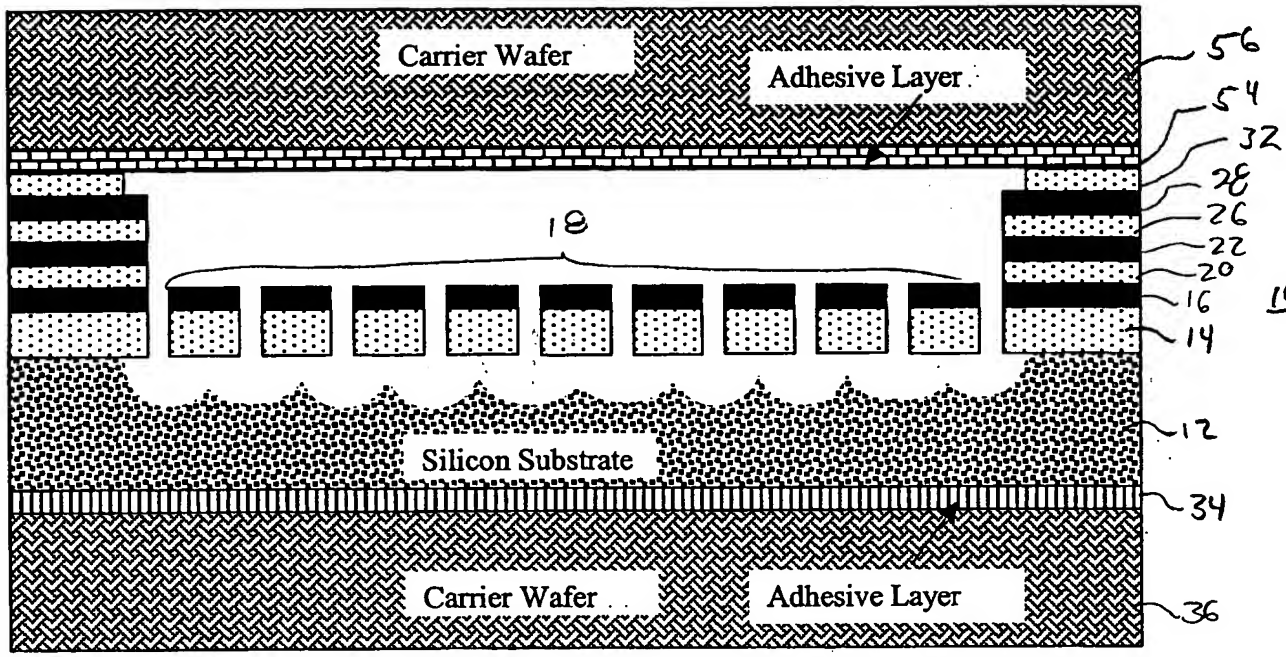

Carrier Wafer
Adhesive Layer
56
54
32
28
26
22
20
16
14
10
18
12
Silicon Substrate
34
Carrier Wafer
Adhesive Layer
36

FIG. 28

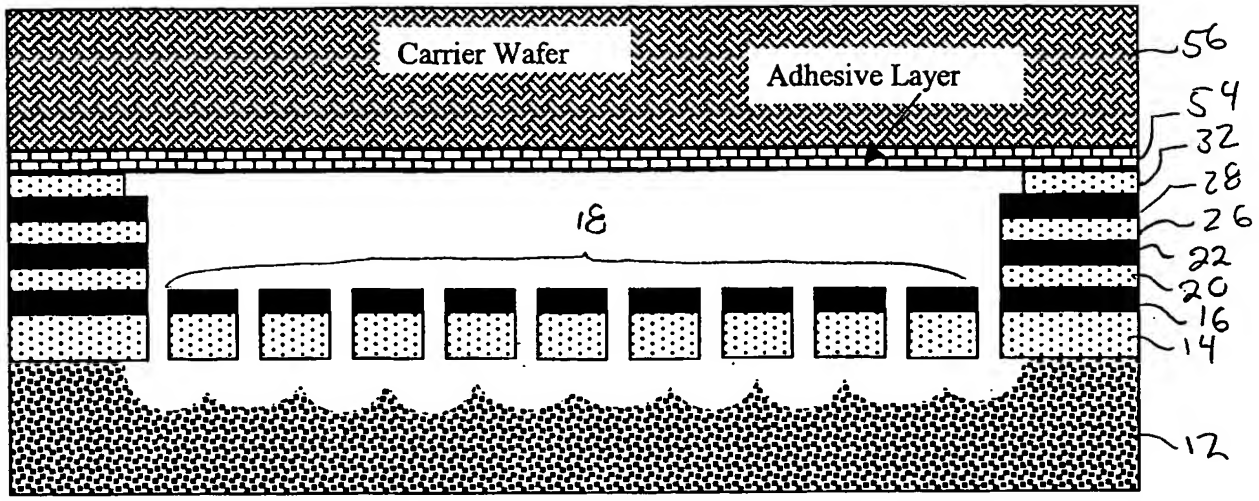

Carrier Wafer
Adhesive Layer
56
54
32
28
26
18
22
20
16
14
12

FIG. 29

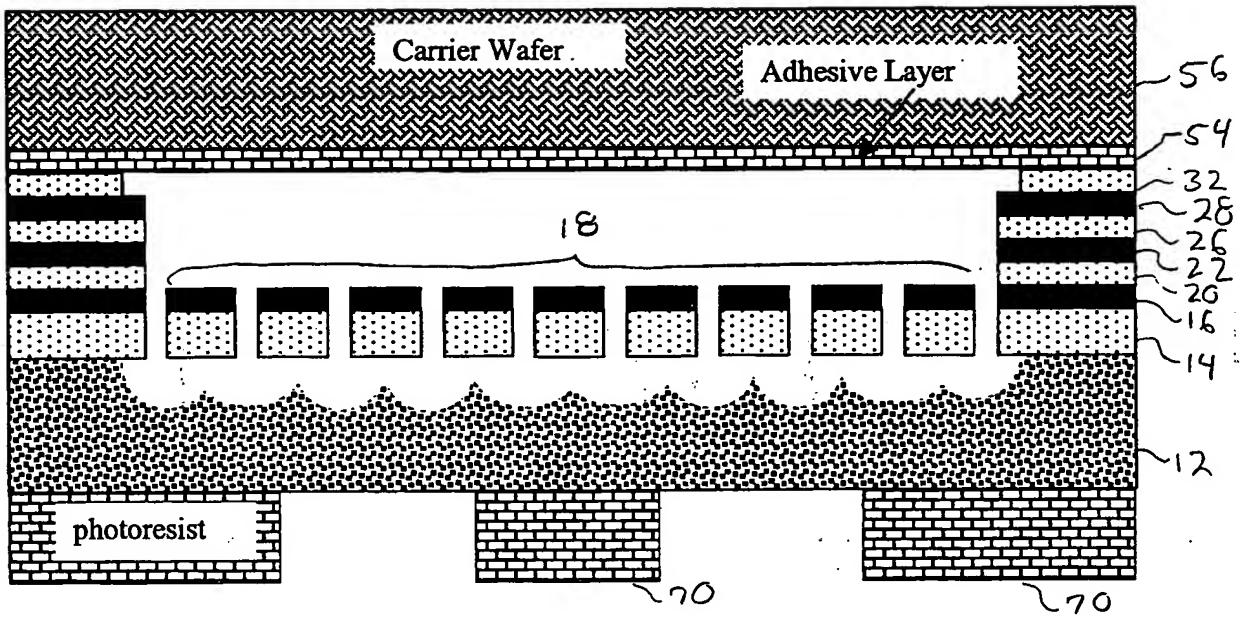

Carrier Wafer
Adhesive Layer
56
54
32
28
26
18
22
20
16
14
12
photoresist
70
70

FIG. 30

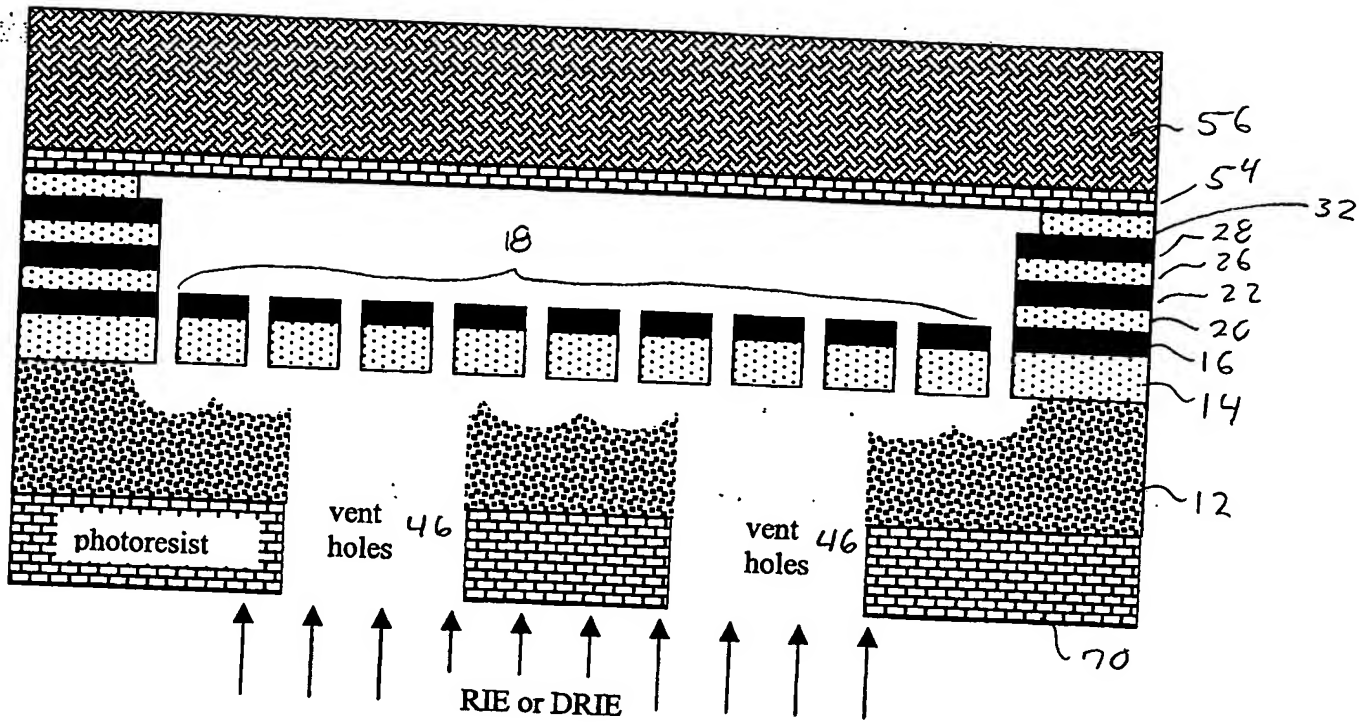

56
54
32
28
26
22
20
16
14
12
18
photoresist
vent holes
46
vent holes
46
70
RIE or DRIE

FIG. 31

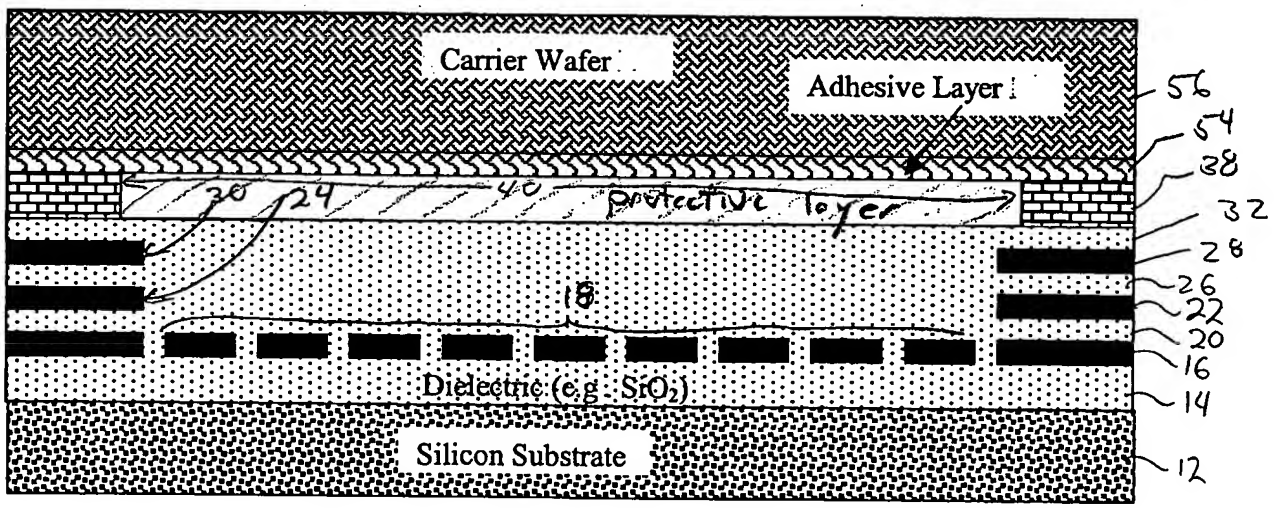

Carrier Wafer
Adhesive Layer
56
54
38
32
28
26
22
20
16
14
12
18
30
24
40
protective layer
Dielectric (e.g. SiO_2)
Silicon Substrate

FIG. 32

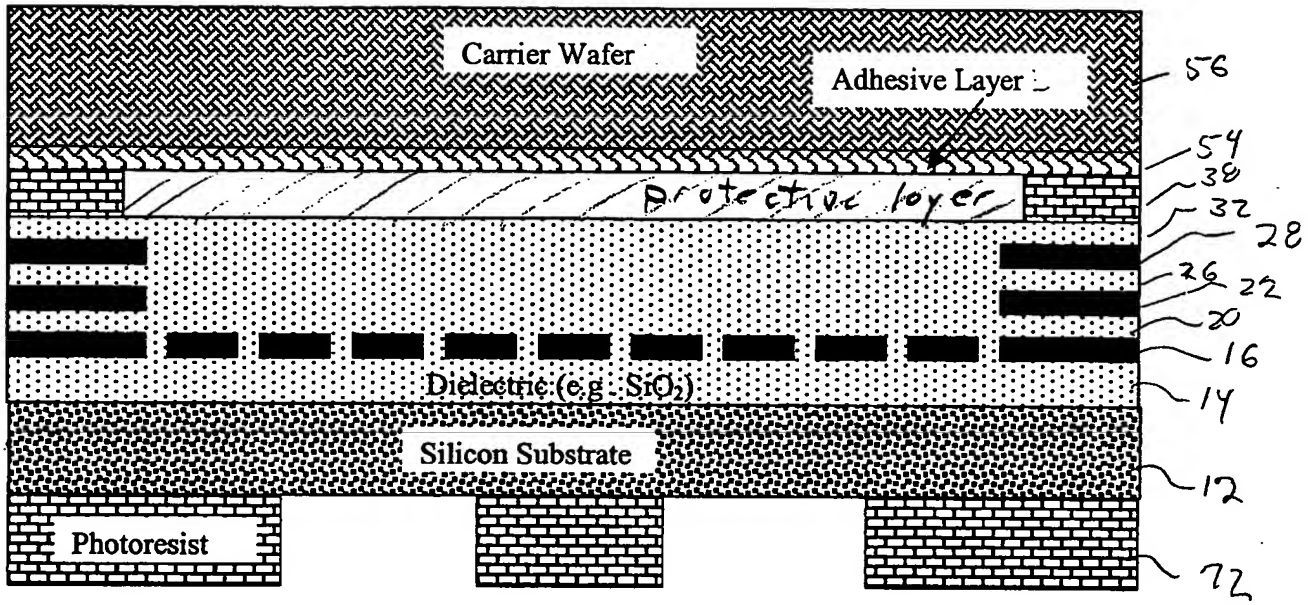
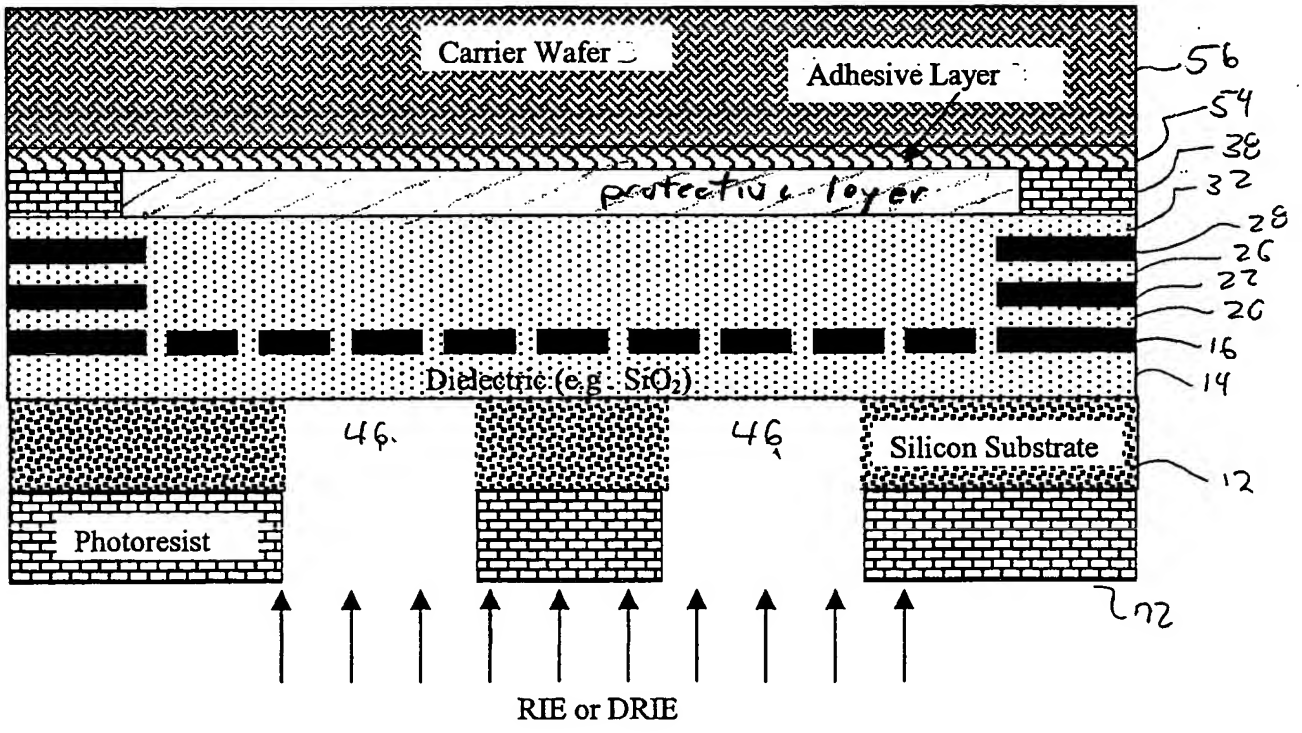

Carrier Wafer
Adhesive Layer
56
protective layer
54
38
32
28
26
22
20
16
Dielectric (e.g. SiO_2)
14
Silicon Substrate
12
Photoresist
72

FIG. 33


Carrier Wafer
Adhesive Layer
56
protective layer
54
38
32
28
26
22
20
16
Dielectric (e.g. SiO_2)
14
46
46
Silicon Substrate
12
Photoresist
72
RIE or DRIE

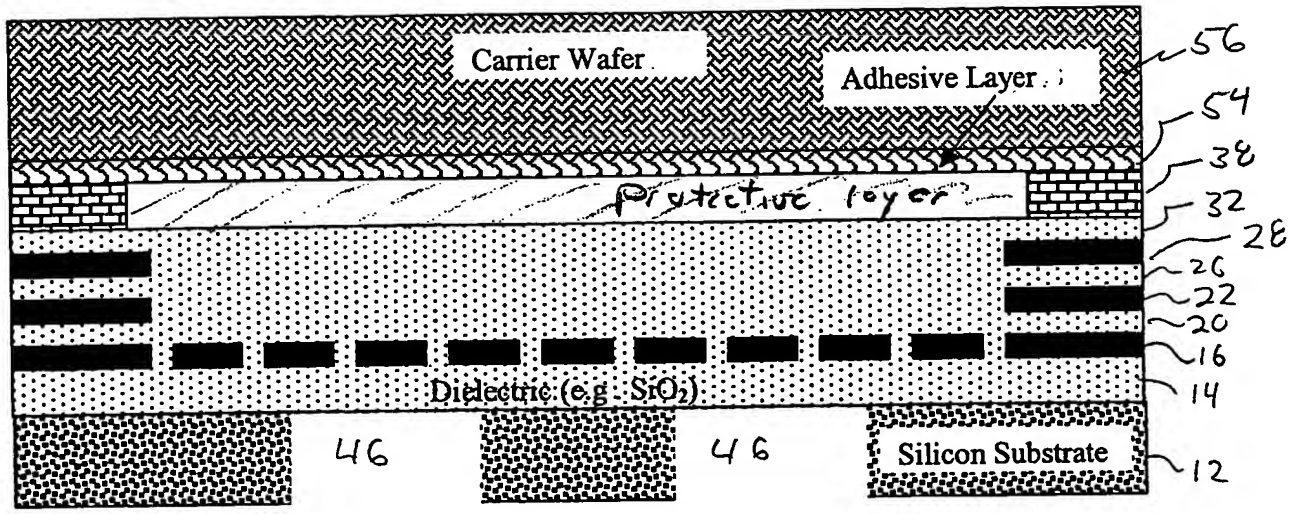

Carrier Wafer
Adhesive Layer
Protective layer
Dielectric (e.g. SiO_2)
46
46
Silicon Substrate
56
54
38
32
28
26
22
20
16
14
12

FIG. 34

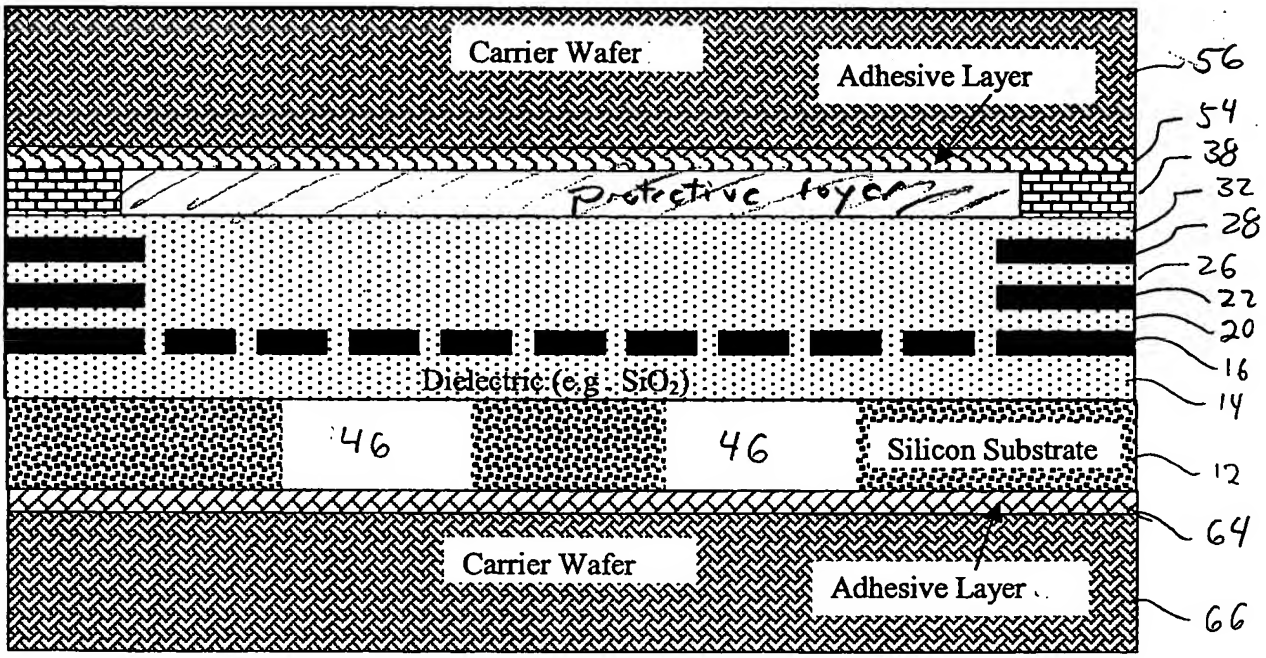

Carrier Wafer
Adhesive Layer
Protective layer
Dielectric (e.g. SiO_2)
46
46
Silicon Substrate
Carrier Wafer
Adhesive Layer
56
54
38
32
28
26
22
20
16
14
12
64
66

FIG. 35

FIG. 36

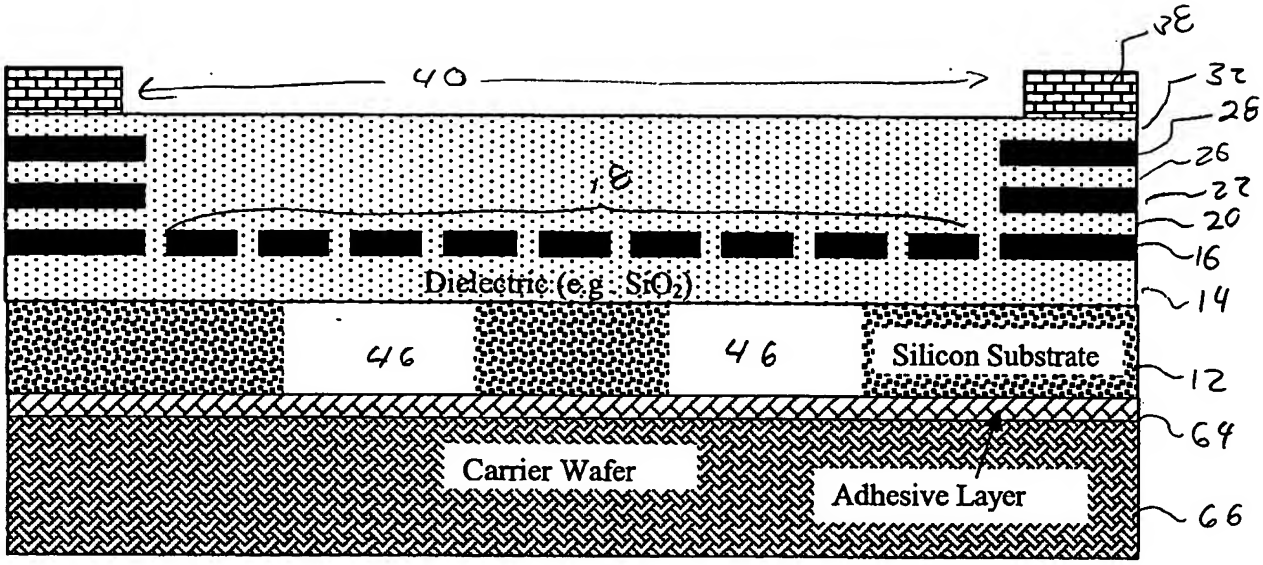


FIG. 37

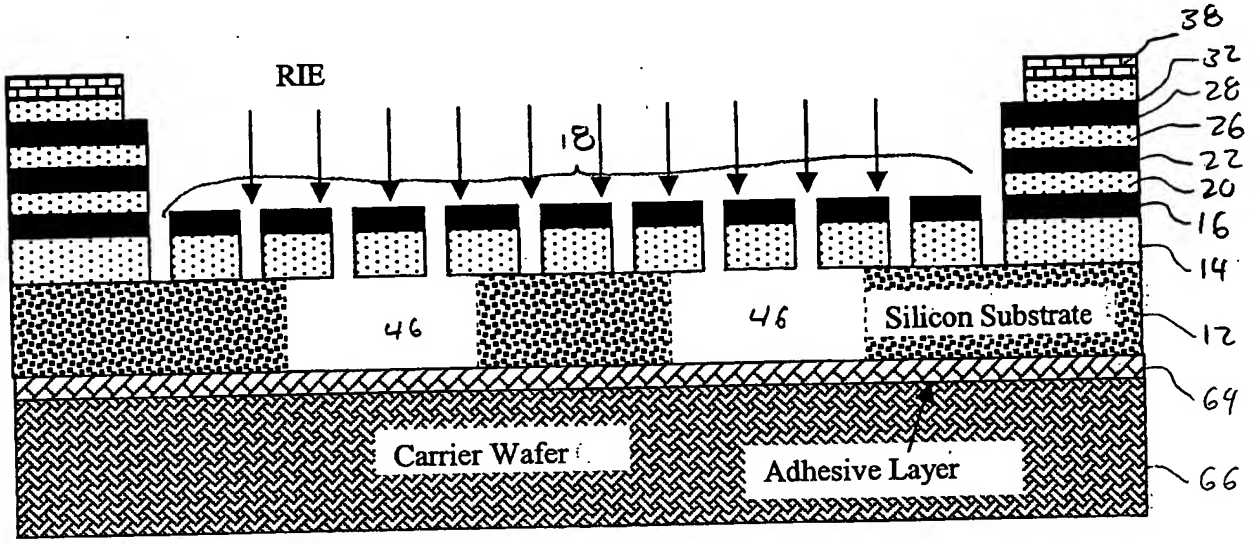


FIG. 38

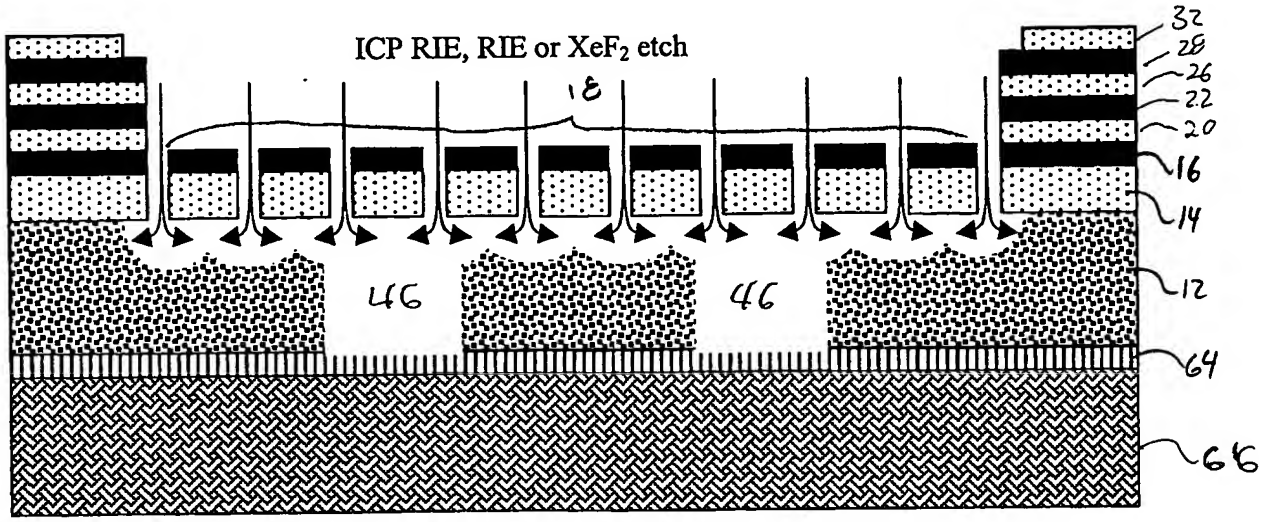


FIG. 39

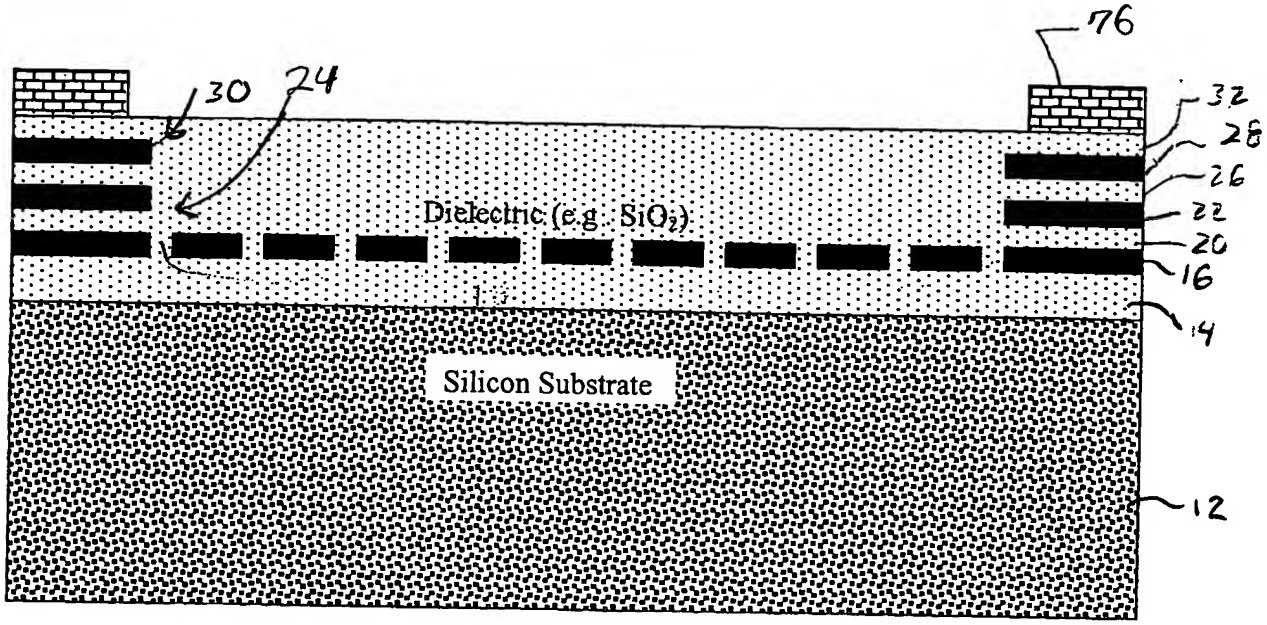

76
30
24
32
28
26
22
20
16
14
Dielectric (e.g. SiO_2)
Silicon Substrate
12

FIG. 40

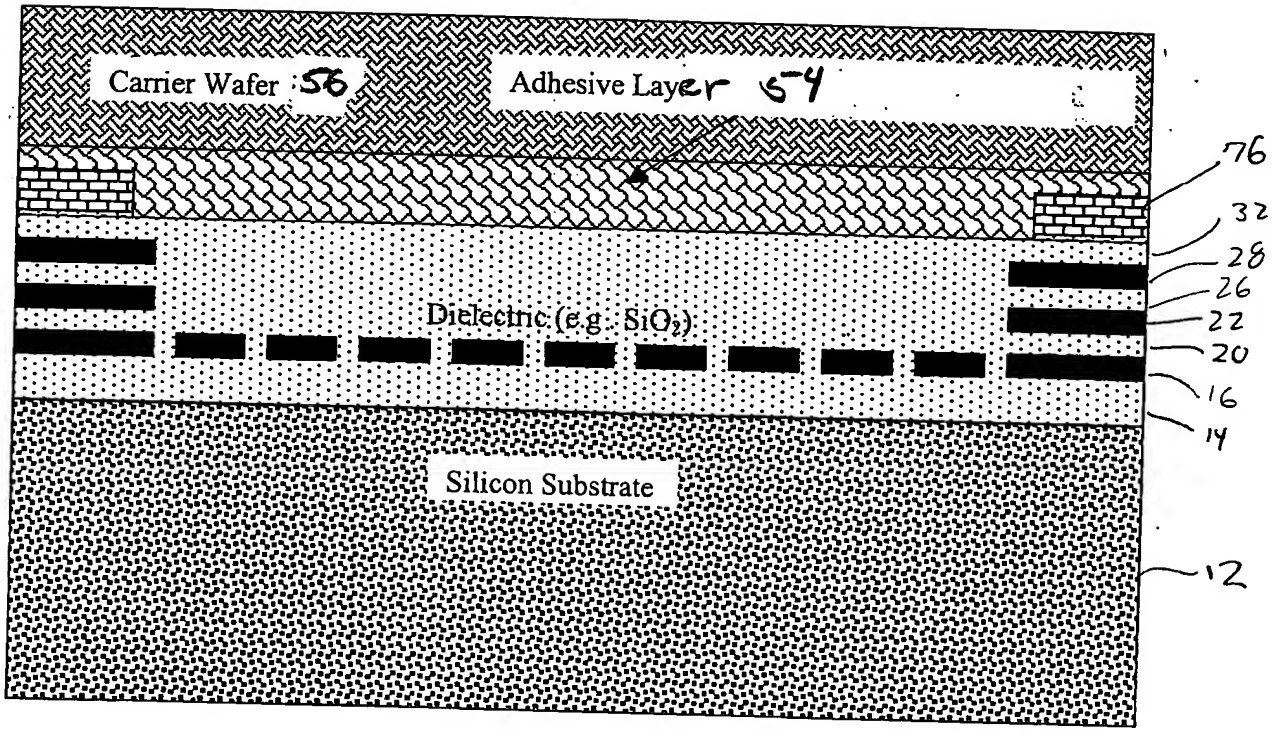

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
Dielectric (e.g. SiO_2)
Silicon Substrate
12

FIG. 41

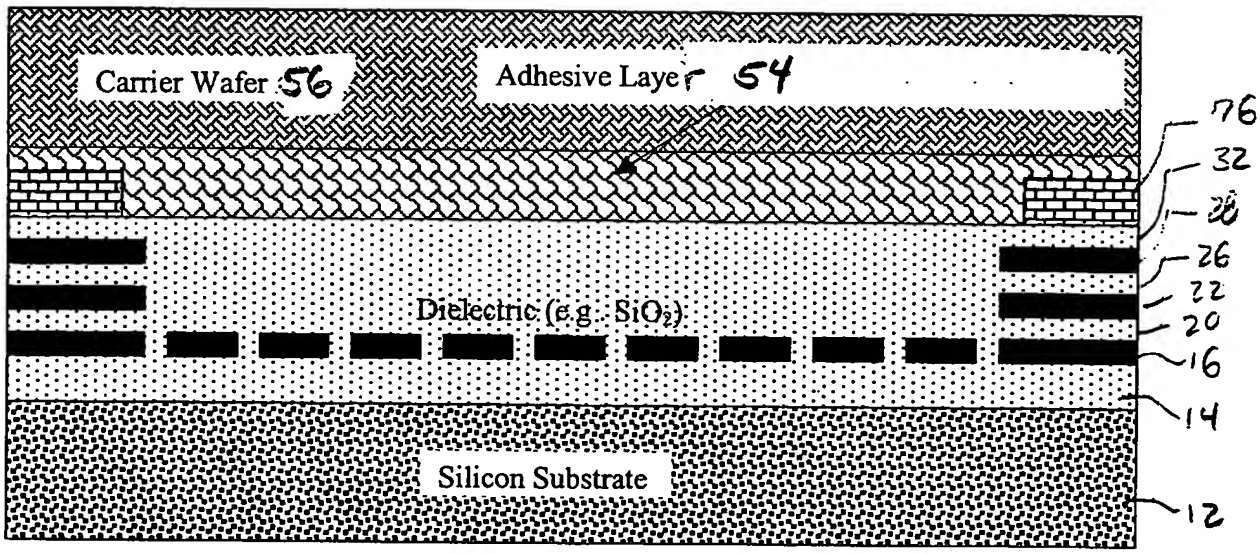

Carrier Wafer 56
Adhesive Layer 54
Dielectric (e.g. SiO_2)
Silicon Substrate
76
32
28
26
22
20
16
14
12

FIG. 42

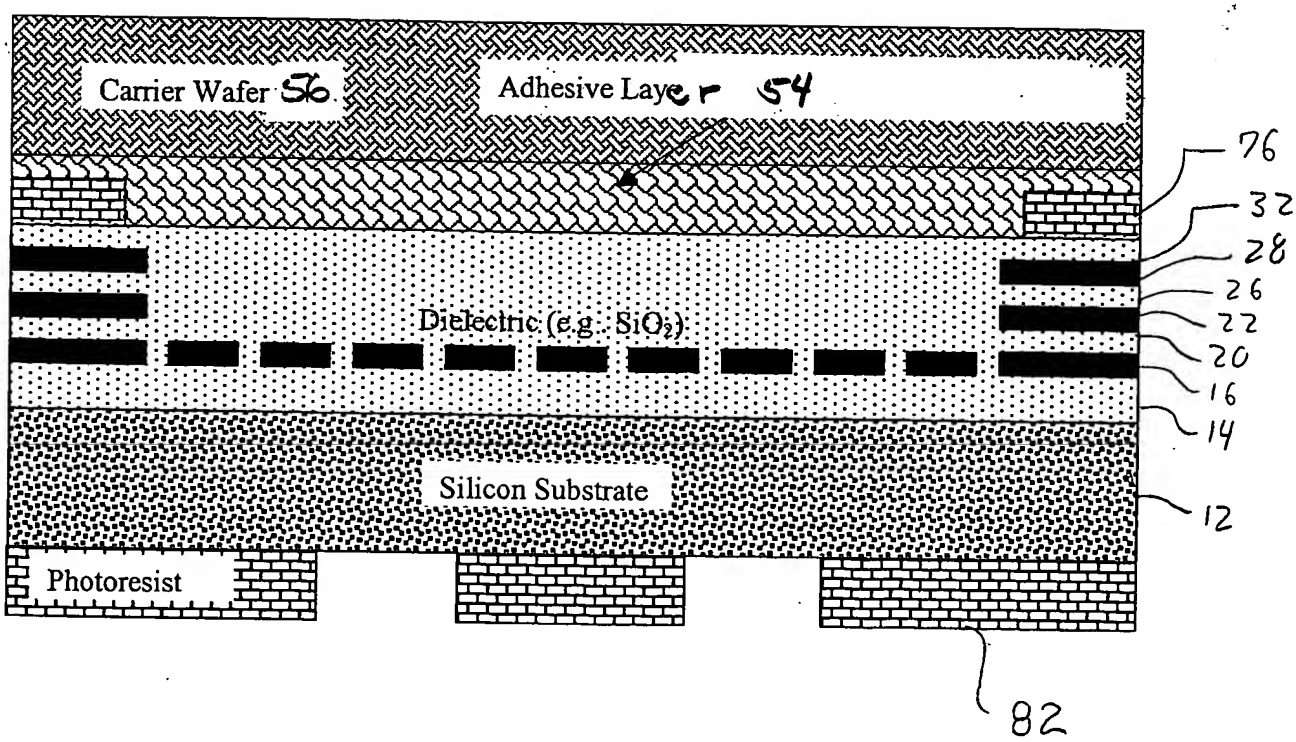

Carrier Wafer 56
Adhesive Layer 54
Dielectric (e.g. SiO_2)
Silicon Substrate
Photoresist
76
32
28
26
22
20
16
14
12
82

FIG. 43

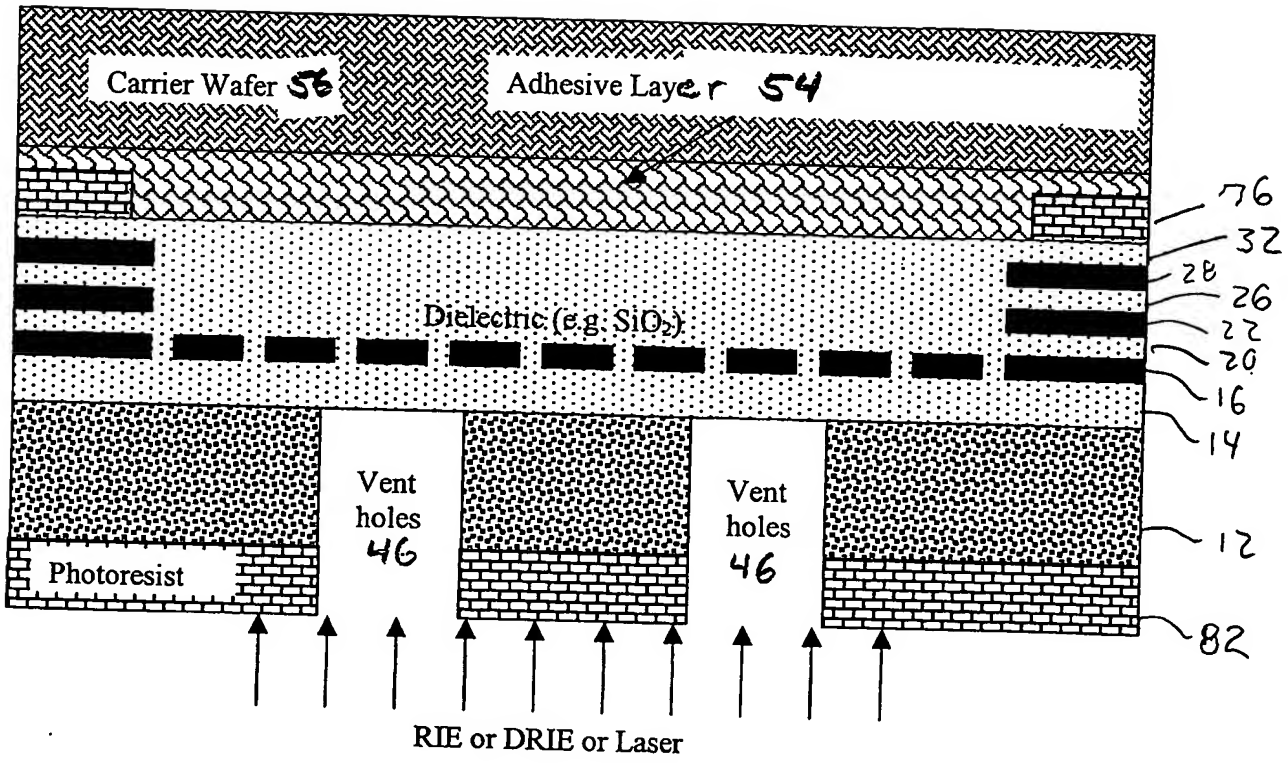
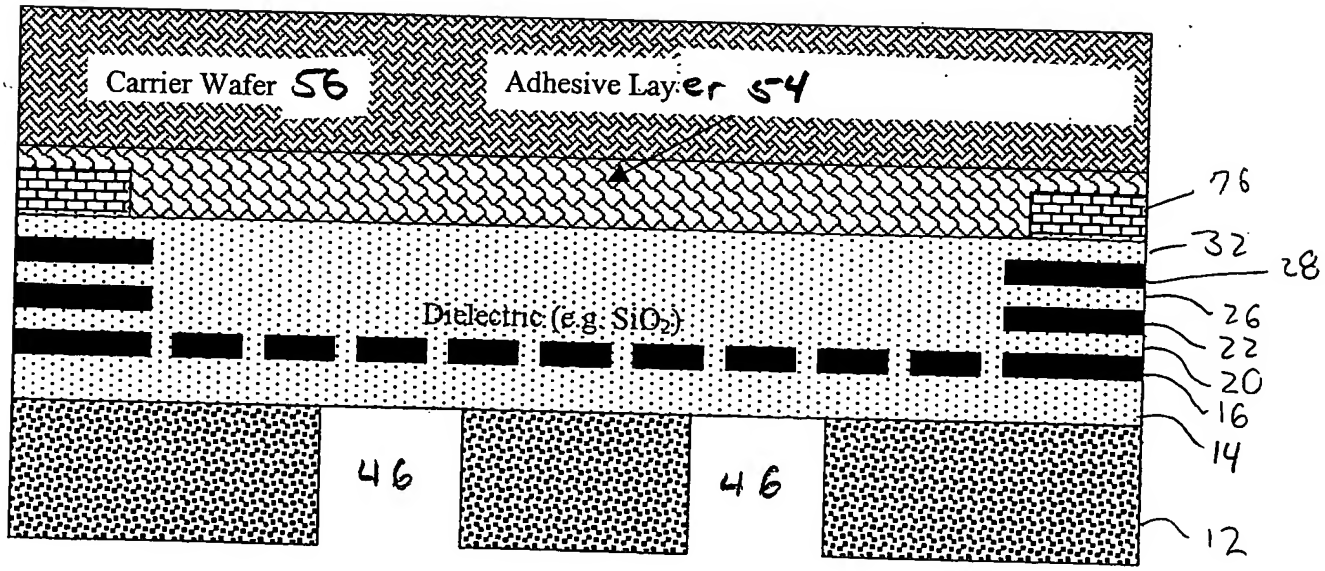

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
Dielectric (e.g. SiO_2)
Vent holes 46
Vent holes 46
12
Photoresist
82
RIE or DRIE or Laser

FIG. 44


Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
Dielectric (e.g. SiO_2)
46
46
12

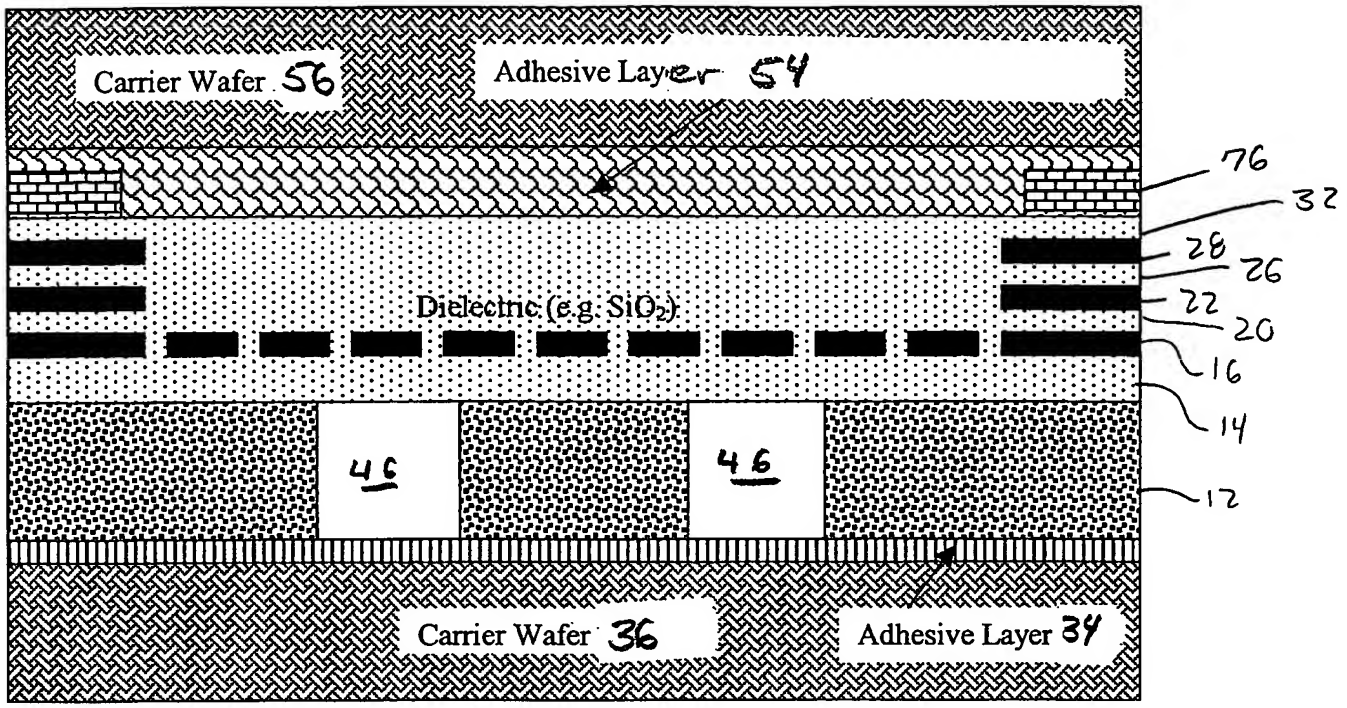

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
Dielectric (e.g. SiO_2)
22
20
16
14
46
46
12
Carrier Wafer 36
Adhesive Layer 34

FIG. 45

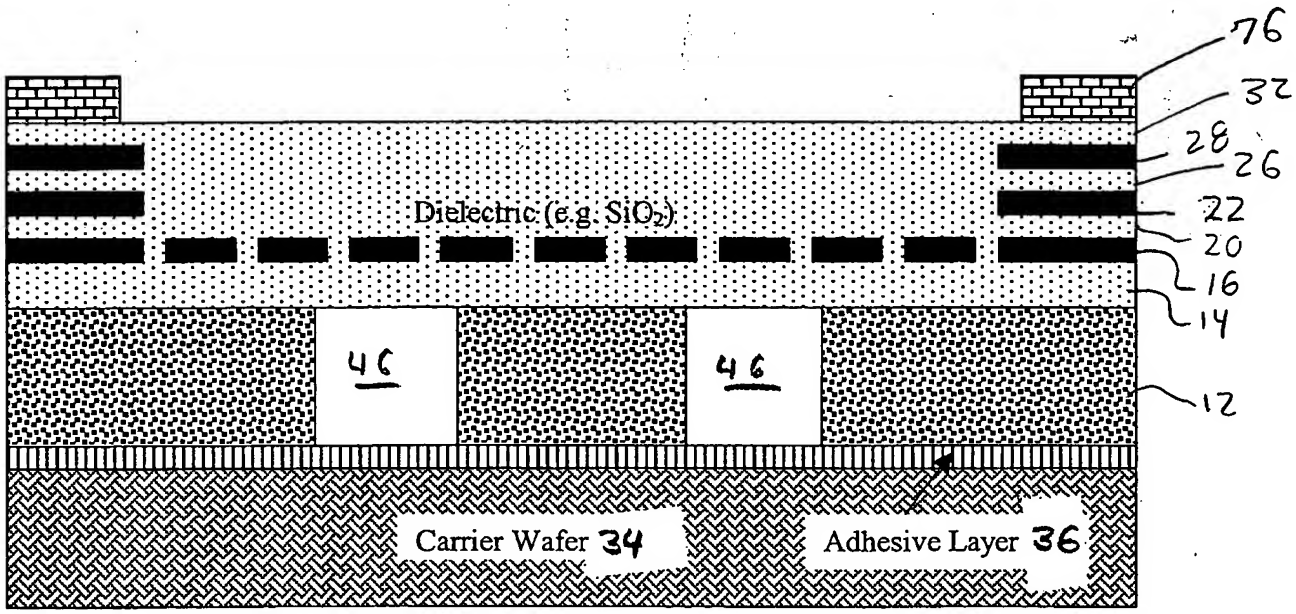

76
32
28
26
Dielectric (e.g. SiO_2)
22
20
16
14
46
46
12
Carrier Wafer 34
Adhesive Layer 36

FIG. 46

FIG. 47

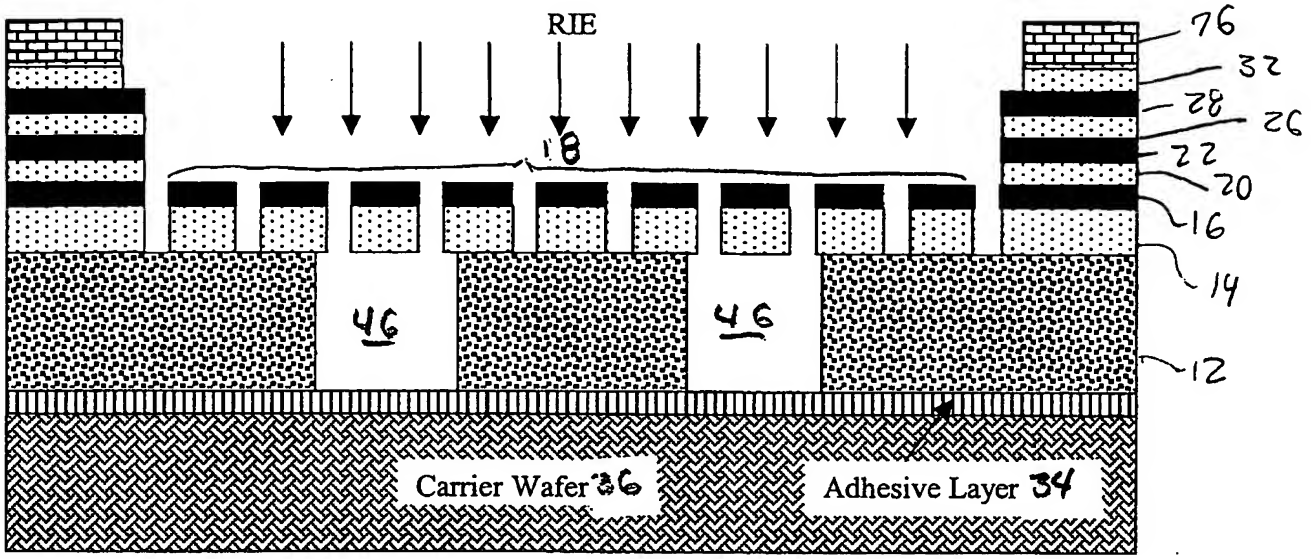
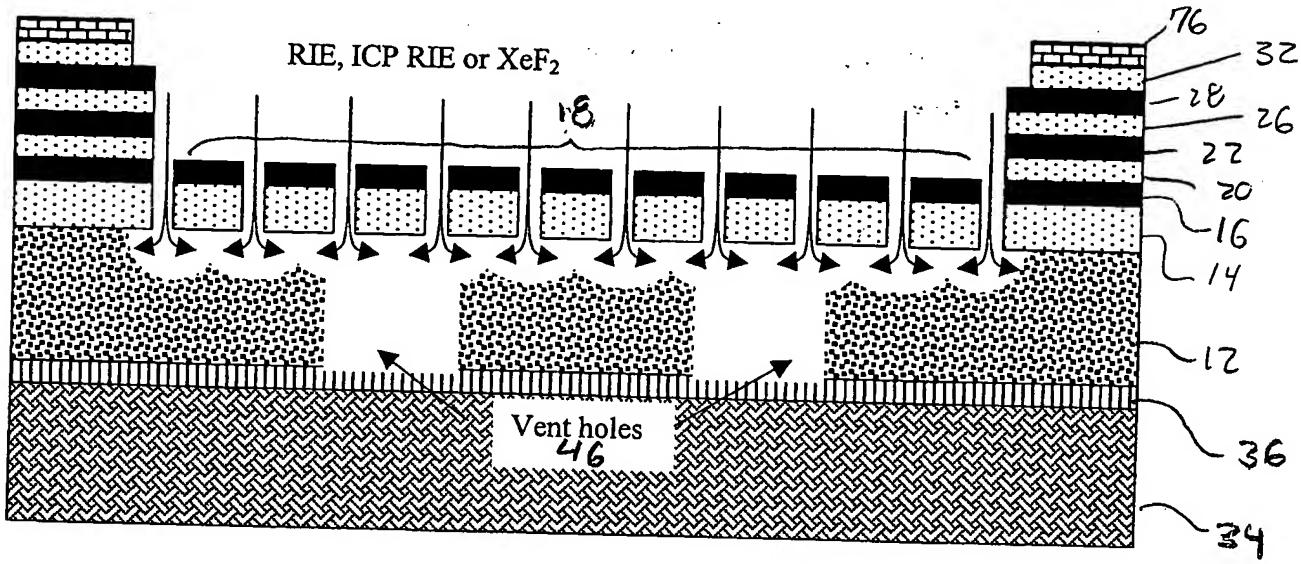

RIE
76
32
28
26
22
20
16
14
12
18
46
46
Carrier Wafer 36
Adhesive Layer 34

FIG. 48


RIE, ICP RIE or XeF_2
76
32
28
26
22
20
16
14
12
18
Vent holes 46
36
34

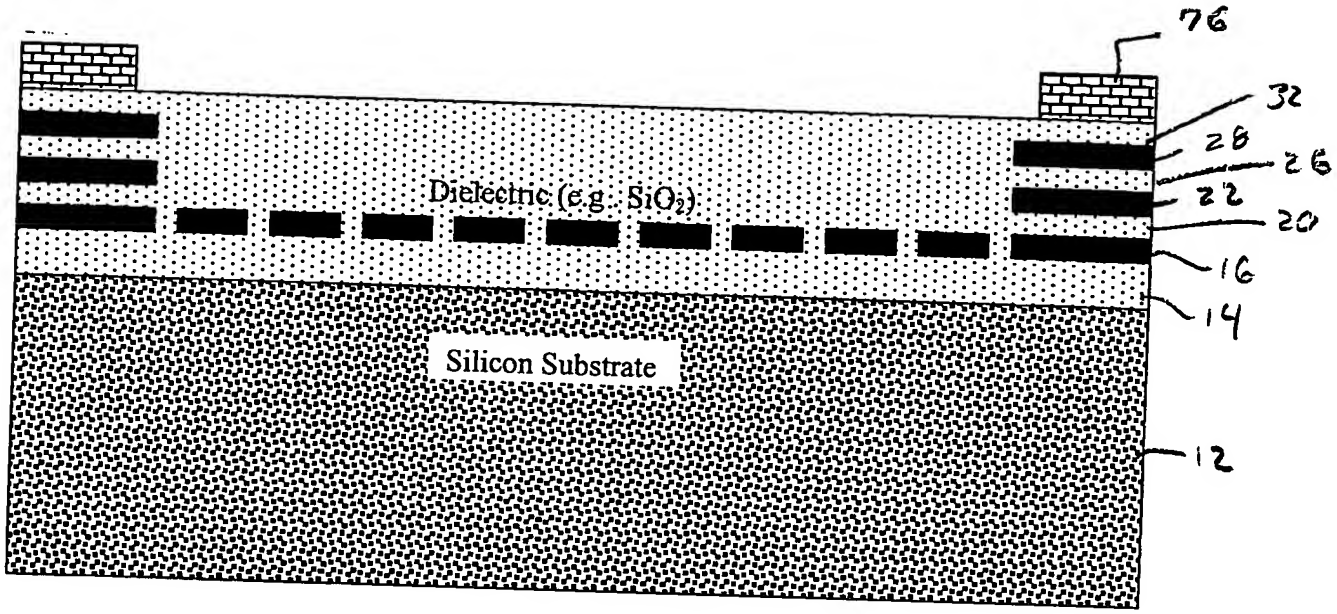

76
32
28
26
22
20
16
14
12
Dielectric (e.g. SiO_2)
Silicon Substrate

FIG. 4J

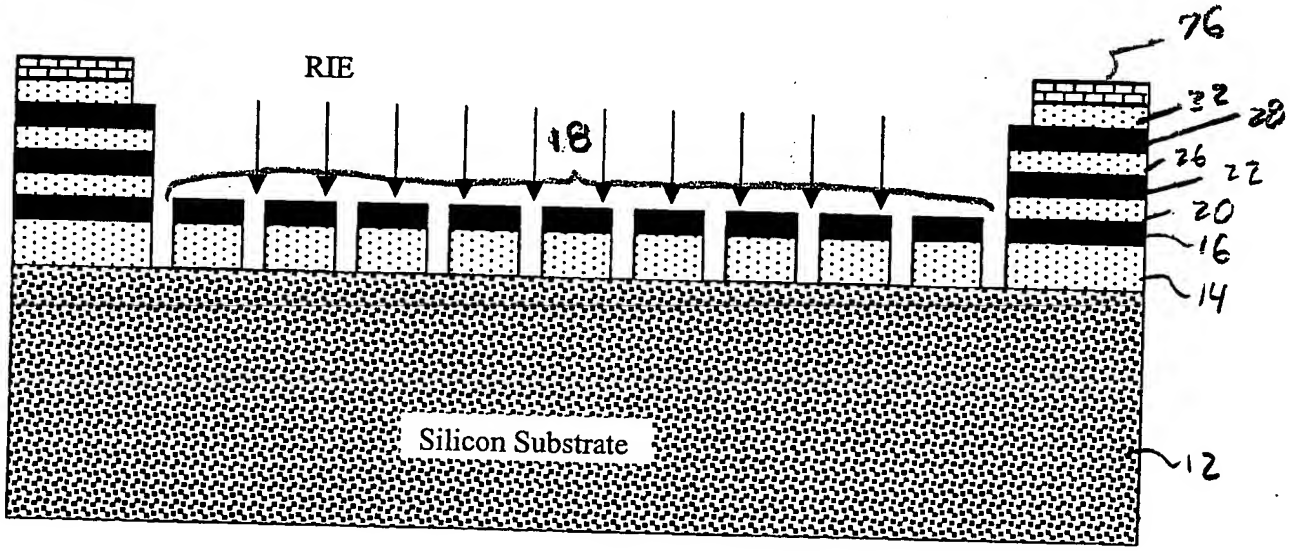

RIE
18
76
32
28
26
22
20
16
14
12
Silicon Substrate

FIG. 5O

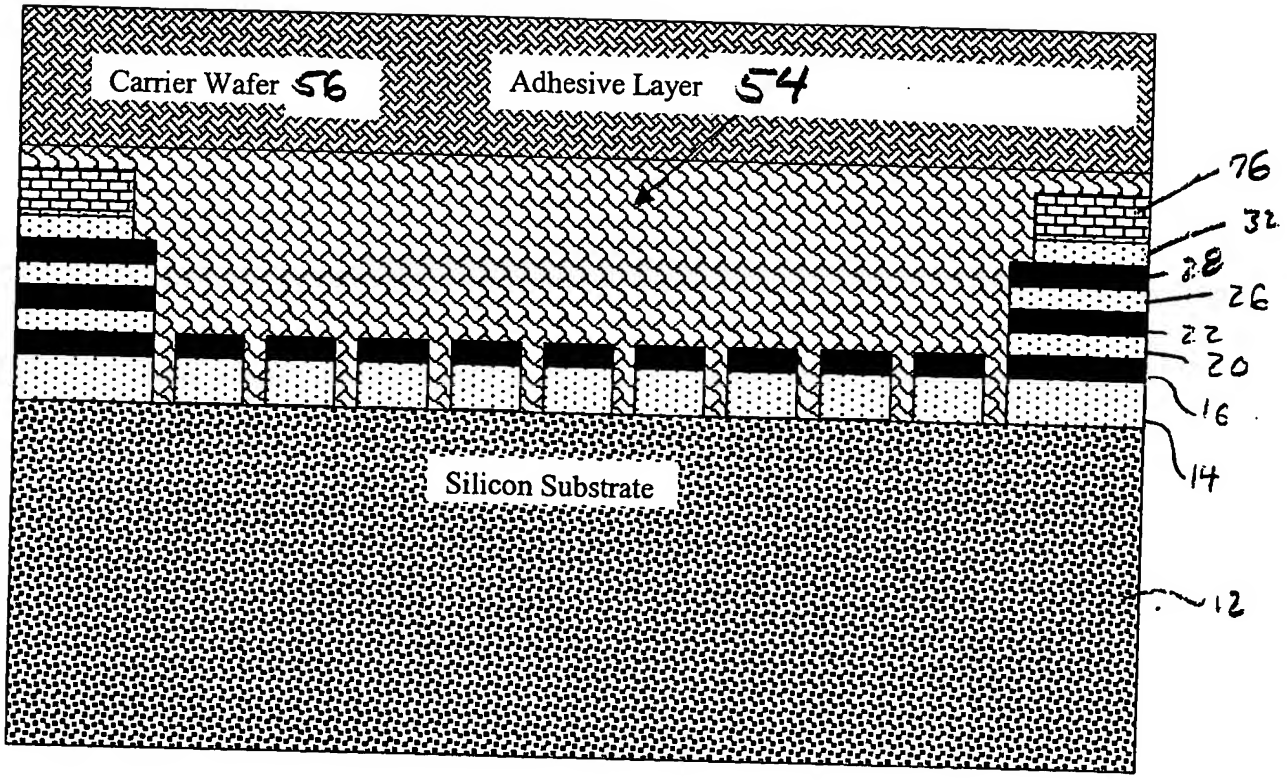

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
Silicon Substrate
12

FIG. 51

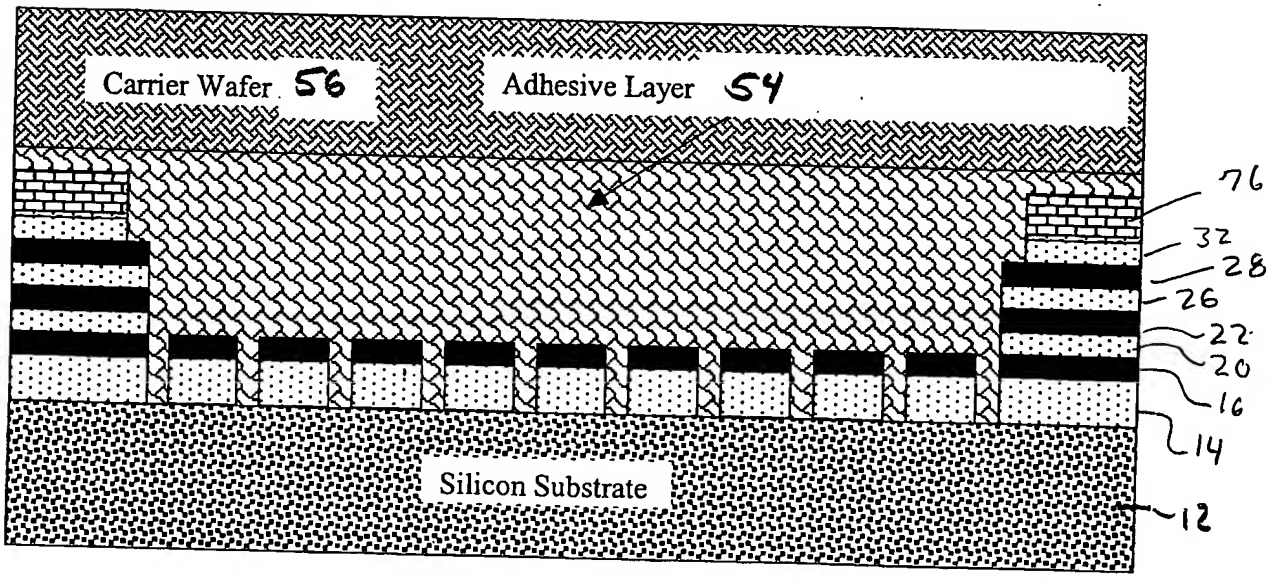

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
Silicon Substrate
12

FIG. 52

FIG. 53

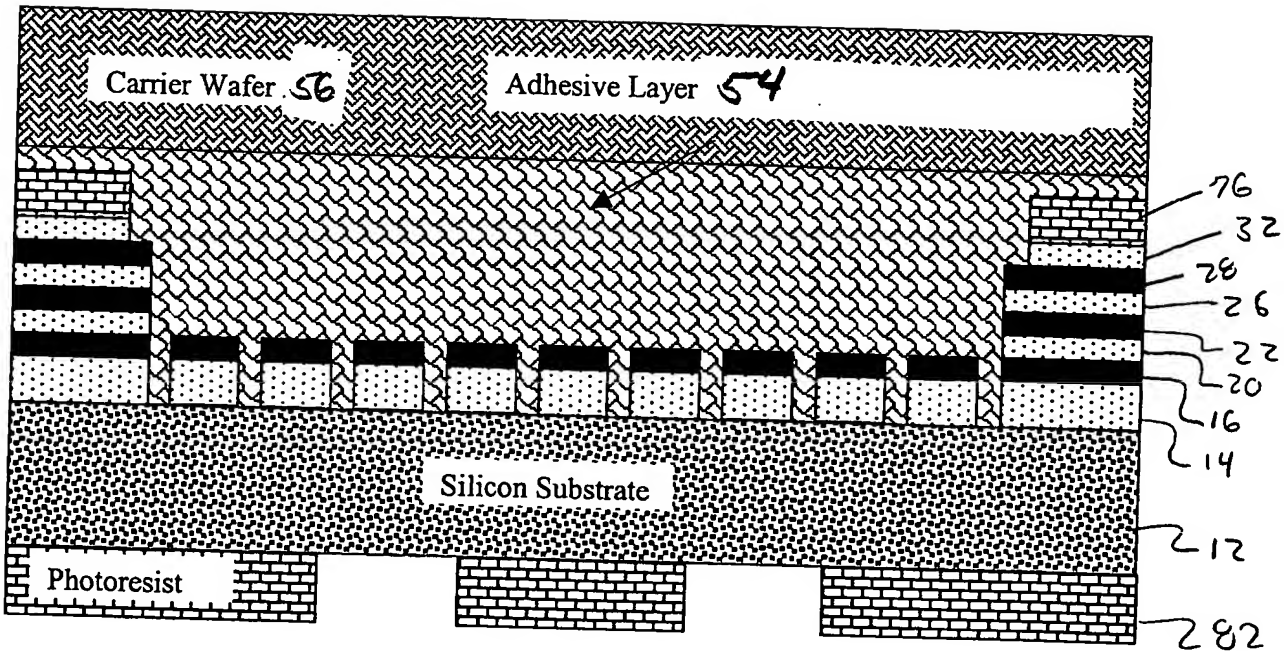

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
Silicon Substrate
12
Photoresist
82

FIG. 54

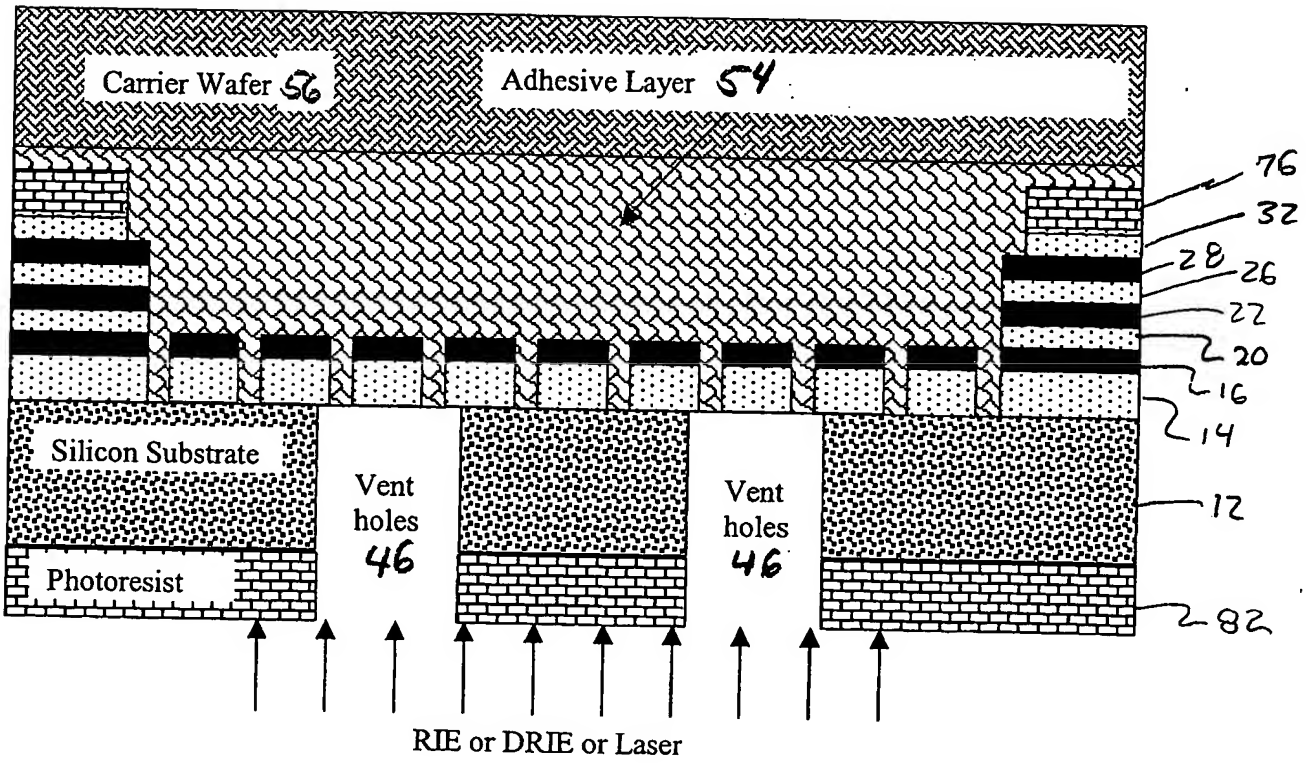

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
Silicon Substrate
Vent holes 46
Vent holes 46
12
Photoresist
82
RIE or DRIE or Laser

FIG. 55

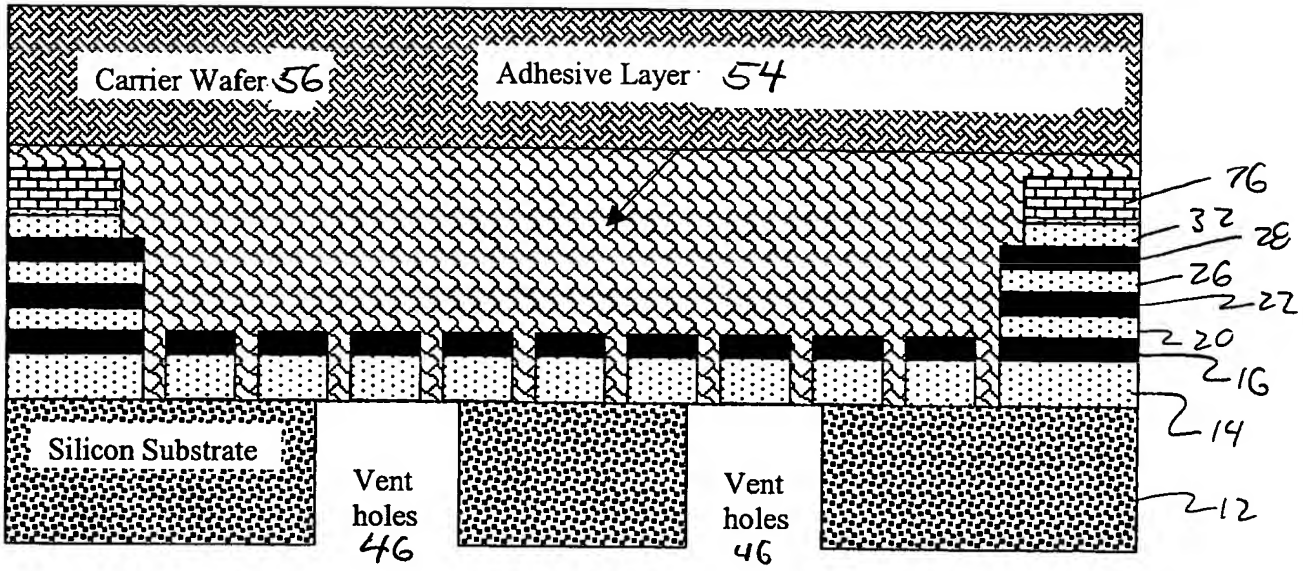

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
12
Silicon Substrate
Vent holes 46
Vent holes 46

FIG. 56

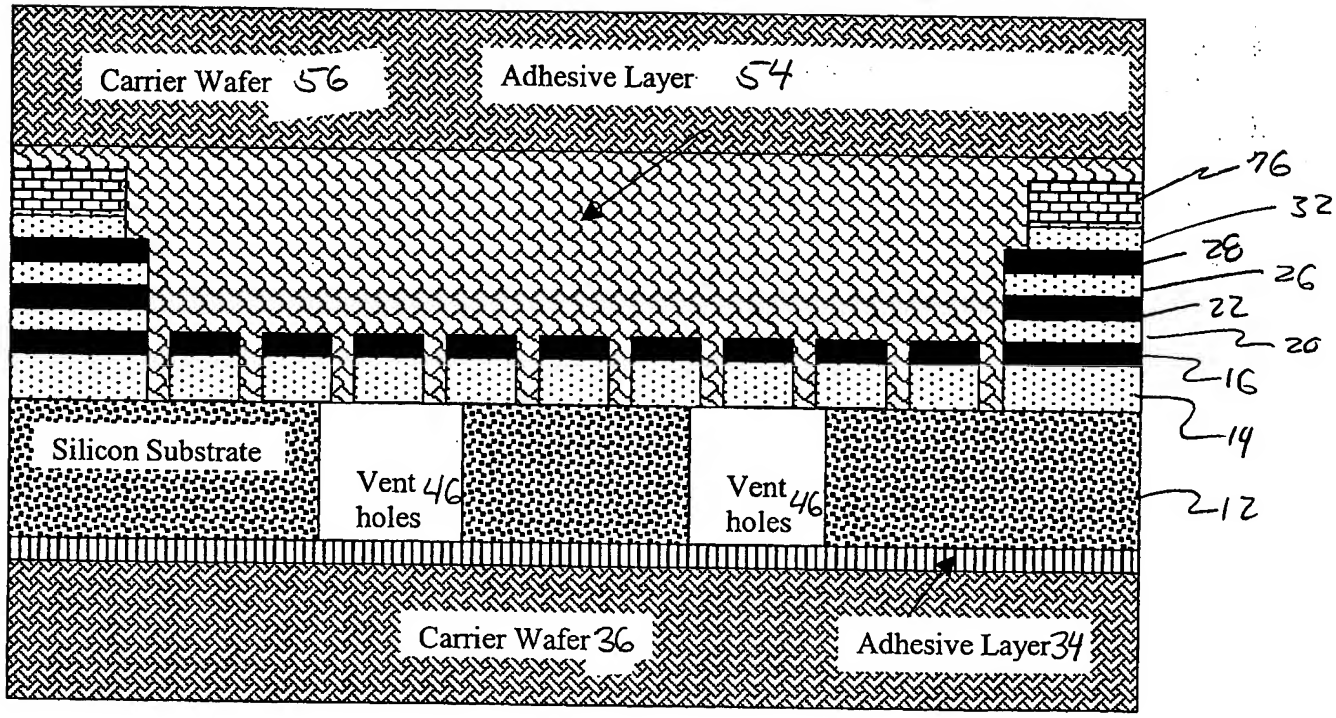

Carrier Wafer 56
Adhesive Layer 54
76
32
28
26
22
20
16
14
12
Silicon Substrate
Vent holes 46
Vent holes 46
Carrier Wafer 36
Adhesive Layer 34

FIG. 57

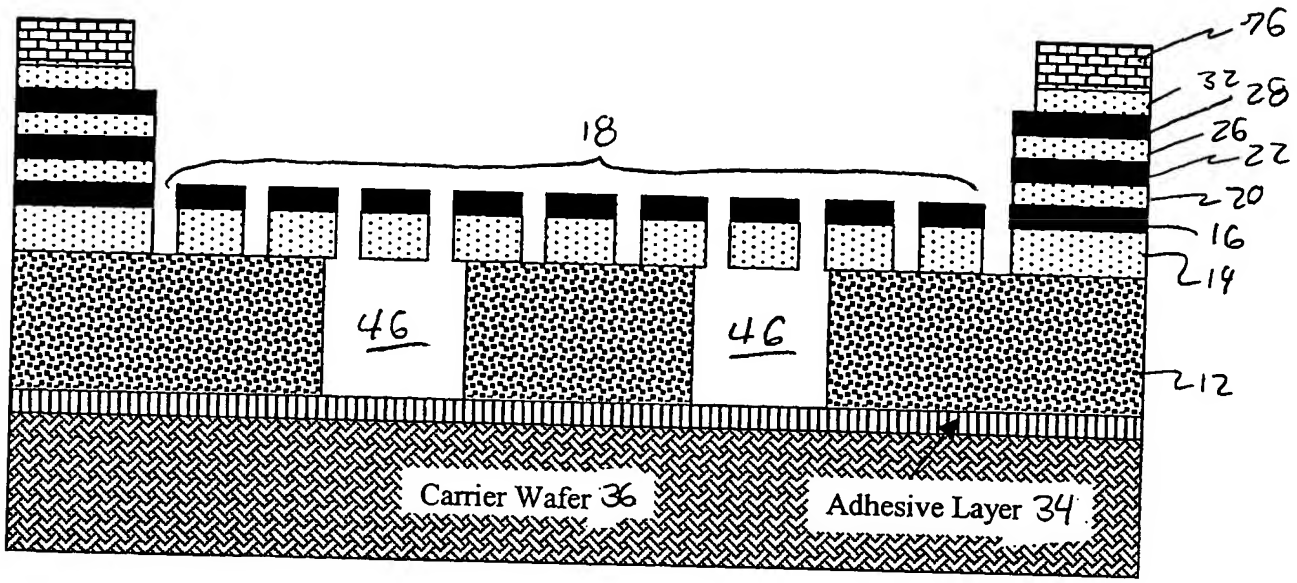
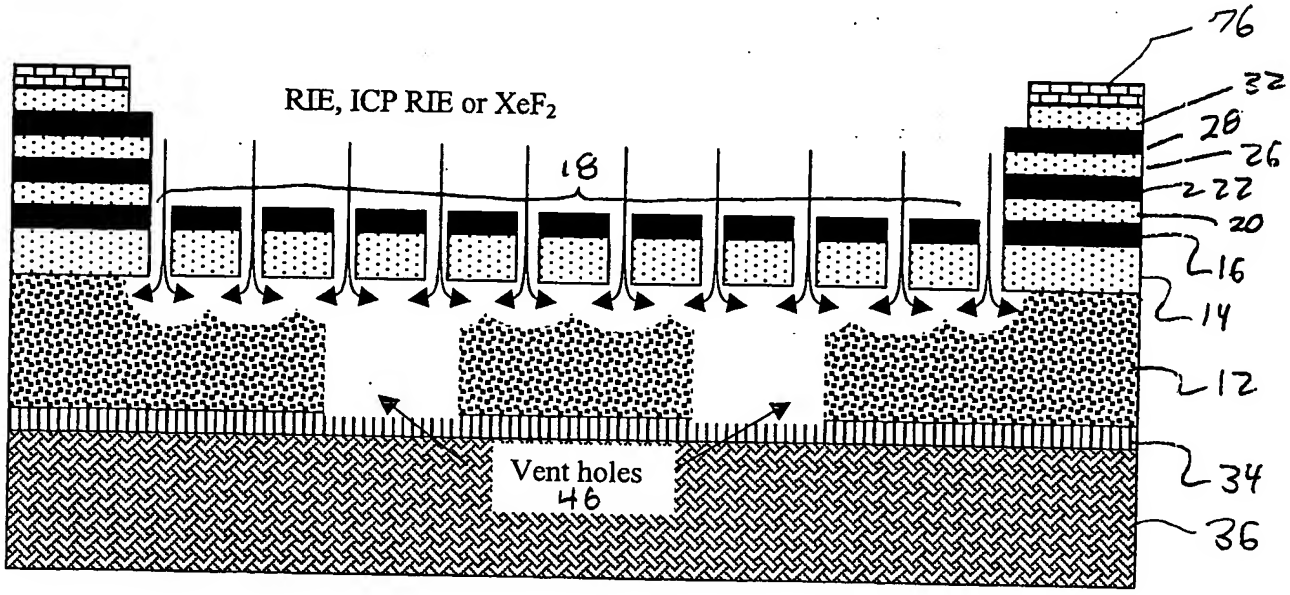

76
32
28
26
22
20
16
14
18
46
46
12
Carrier Wafer 36
Adhesive Layer 34

FIG. 58


76
RIE, ICP RIE or XeF_2
32
28
26
22
20
18
16
14
12
Vent holes
46
34
36